# CMOS Logic MN4000B Series CMOS Digital IC CMOS Logic MN4000B

**Panasonic** 

### Index Table/Selection Guide by Function

Explanation

**General Specifications** 

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#### **PREFACE**

The CMOS logic IC MN4000B series data book has been published to meet consummer needs as the revised edition of the current MN4000B series by expanding the range and adding rew products. The MN4000B series are general purpose CMOS devices which provide various functions and find applications in both consumer and industrial fields.

General purpose CMOS LOGICS have features such as low power dissipation, single power supply, wide operation range of power supply, high noise immunity and high integration, all of which are superior to conventional DTL, TTL and LS-TTL.

The increase of CMOS suppliers in recent years resulted in the necessity for compatibility with respect to electric characteristics and functions. We have begun to market the MN4000B series for the general purpose CMOS LOGICS stipulated by IEC/JEDED. We hope you will make use of these devices as well as other Matsushita semiconductors.

July, 1984

Matsushita Electronics Corporation

Semiconductor Division

The application circuits in this book have been chosen as examples of the characteristics and performance of our products. The information contained herein is believed to be reliable. However, no responsibility is assumed for any consequence of its use, nor for patent liability with respect to the use of the information. The device specifications are subject to change without prior notice.

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# Explanation



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#### **Explanation**

#### 1. General descriptions of MN4000B series data

The MN4000B series are fully buffered digital ICs which meet IEC/JEDEC stipulations. The MN4000B series are designed for pin compatibility with CMOS4000 and 4500 which are used over a wide range.

The MN4000B series make system designing simple beause output characteristics are standardized.

#### **CMOS** features

- Low power dissipation: 10 nW typ./gate (static)
- Wide range of operating voltage: +3V ~ 15V
- Wide range of operating temperature: −40 ~ +85°C
- High DC fanout: 50 typ.
- All series include the output buffer (capable of driving 1 LS-TTL)
- Protection circuit for static voltage to input and output
- High speed (higher than conventional CMOS4000B)
- High integration
- · High noise immunity

#### 2. CMOS Basic circuit · Cross-sectional view

As a representative of the MN4000B series, basic conceptions of the inverter are described below.

The CMOS inverter is constructed with a MOS P-channel transistor  $(P_1)$  and N-channel transistor  $(N_1)$  of the enhancement type; the connecting gates are for input and the connecting drains are for output (illustrated in Fig. 1). The source of the P-channel MOS transistor is connected to  $V_{DD}$  (+) and that of the N-channel MOS transistor is connected to  $V_{SS}$  (-).

Let us consider the output voltage ( $V_O$ ) if the input voltage ( $V_I$ ) changes between  $V_{SS}$  and  $V_{DD}$ .

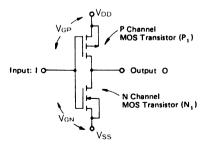


Fig. 1 CMOS Inverter

#### 2.1 If input is VSS level

 $P_1$  switches on because the  $V_{GP}$  of  $P_1$  (gate-source voltage) is deep negative bias.  $N_1$  switches off because the  $V_{GN}$  of  $N_1$  (gate-source voltage) is zero.

Though the output voltage is determined by the ratio of  $P_1$  and  $N_2$  resistance, it almost becomes  $V_{DD}$  due to some  $k\Omega$  for the ON-side transistor and hundreds of  $M\Omega$  for the OFF-side transistor. Less current flows between  $V_{DD}$  and  $V_{SS}$ .

#### 2.2 For intermediate voltage between VSS and VDD.

#### $V_{DD}$

The output (0) is a medium level divided by both  $P_1$  and  $N_1$  ON resistor values. In this case, the output level goes nearly to  $V_{DD}$  when the input voltage  $(V_I)$  is around  $V_{SS}$ , and it comes down to  $V_{SS}$  when around  $V_{DD}$ . Current flows between  $V_{DD} \sim V_{SS}$ .

#### 2.3 If input is V<sub>DD</sub> level

 $P_1$  switches off because the  $V_{GP}$  of  $P_1$  is zero and  $P_2$  switches on because the  $V_{GN}$  is  $V_{DD} \sim V_{SS}.$  This is a counter-action of 2.1 and the output (0) voltage is almost  $V_{SS}.$ 

Less current flows between V<sub>DD</sub> and V<sub>SS</sub>. Fig. 2 shows that current flows only at the transient time shown by the dotted line when the state of the inverter changes where the horizontal axis represents the input voltage and the vertical axis represents the output voltage.

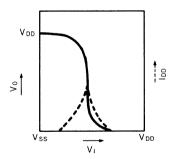


Fig. 2 Inverter Input/Output Voltage Characteristics

Fig.3 shows the cross-sectional view of the CMOS inverter. The P-N junction is used for isolation between P-channel and N-channel MOS transistors to make the CMOS inverter on a single silicon substrate.



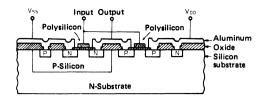
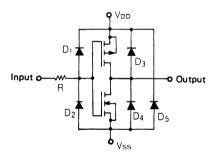


Fig. 3 CMOS Inverter Cross-Sectional View

Fig. 3 shows the views to make an N-channel MOS transistor in a P-well region after making it on an N-type silicon substrate.

Because the N-type substate is connected to  $V_{DD}$  and the P-well to  $V_{SS}$ , each P-channel and N-channel transistor can be operated electrically independent due to reverse biases when the power is applied. This construction of the CMOS circuit form the parasitic diode shown in Fig. 4. It is important to use with in the maximum rating because exceeding the forward current of the diode may damage the IC.



R : Input Protection Resistor

D<sub>1</sub>: Input Protection Diode

Da : P-channel Transistor

Parasitic Diode by Forming Drain

D<sub>4</sub>: N-channel Transistor Parasitic Diode by Forming Drain

D<sub>5</sub>: Parasitic Diode by Forming P-well

Fig. 4 Equivalent circuit of CMOS Inverter with Parasitic Element

Input protection diodes  $D_1$  and  $D_2$  in the equivalent circuit are to protect CMOS inputs against static electrical damage; these are included in all MN4000B series.

#### 3. Designing notes

CMOS logic which has an integration as large as SSI or MSI finds applications in an extensive area. There are specific circuits such as bidirectional analog switches in CMOS technology and many LSIs developed due to small chip size and high integration.

Table 1 Characteristic Comparison Between TTL and CMOS

Item	Normal	LS-TTL	CMOS 4000			
Item	TTL	LS-11L	5V	10V	15V	
Transfer Time (C <sub>L</sub> = 15pF)	10 ns	10 ns	40 ns	20 ns	15 ns	
Flip-Flop Clock Frequency	35 MHz	45MHz	8 MHz	16 MHz	20 MHz	
Quiescent Power	10 mW	2 mW	10 nW	10 nW	10 nW	
Noise Immunity	1V	0.8V	2.25V	4.5V	6.75V	
Fan-out	10	10	50	50	50	

#### 3.1 Supply Voltage Range

CMOS logic of MN4000B series is guaranteed to function ranging from 3V to 15V. It is not guaranteed under 3V because of the increase of propagation delay time (decrease of speed), the increase of output impedance and the loss of noise immunity. It is also not guaranteed over 15V becuse of the increase of dynamic power dissipation, the spike noise exceeding tolerable voltages and other causes which may cause the latch-up and result in damage to the device unless the current is restricted to minimum. Please refrain from using at over 15V.

The level conversion between TTL and CMOS which have different supply voltages can be realized by using the MN4049B or MN4050B.

#### 3.2 Output with Buffer

The MN4000B series have fully buffered output in order to shorten the propagation delay time and to standardize the propagation delay time and characteristics of output driving (Fig. 5). Buffered outputs increase the voltage gain, the static noise immunity and can improve the dynamic noise margin because they have ideal transfer characteristics and low impedance at the output (Fig. 6). The high gain also provides good pulse shaping due to less effect of the input rise or fall time. (Fig. 7 (a) (b).

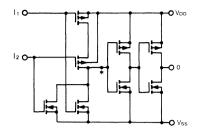


Fig. 5 Typical 2 Input NOR Gate Incorporating Buffer Output Circuit (\*Output for the types without buffer)

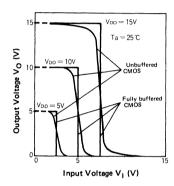


Fig. 6 Transfer Characteristics

Buffered CMOS shows better transfer characteristic.

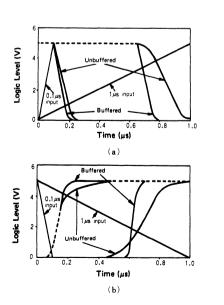


Fig. 7 Output Transfer Characteristics Not Affected by Rise (a) and Fall (b) of Input

#### 3.3 Power Consumption

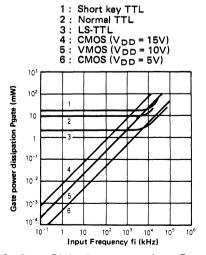
The CMOS is an ideal logic circuit for battery operation because the power consumption in the static state is very low and its operation ranges are very wide.

In the static state, only leakage currents flow through the  $V_{\rm DD}$  to  $V_{\rm SS}$  because the P-channel transistors are not ON simultaneously. The leakage currents are 0.5nA for each gate and the power consumptions are only 2.5nW (5V operation).

It is estimated that more energy is consumed to charge or discharge capacitances (on-ship parasitic capacitances and load capacitances) when the input data or input clock changes during CMOS operations. Actually there is a time when both P-channel and N-channel transistors are ON simultaneously. The dynamic power consumption  $P_{\rm DYN}$  may increase proportionally to the product by the factors of the input clock frequency, loading capacitance ( $C_{\rm L}$ ) and the square of supply voltage ( $V_{\rm DD}$ ). (Refer to formula (1).)

$$P_{DYN} = f \cdot C_L \cdot V_{DD}^2 \cdot \dots (1)$$

The power consumption of CMOS gate is higher than that of LS-TTL in the range from 500 kHz to 2 MHz shown in Fig. 8. However, it is not so much higher for high-integrated CMOS ICs (MSI). The gates switched actually are so few that the power consumption does not increase because most gates are driven at lower clock frequency. It is necessary to analyse or consider the switching speeds of each gate in the circuit when you are to compare the power consumption of the logic devices which have various kinds of process technology. The maximum of static currents (I<sub>DD</sub>) is limited in the general or individual specifications. Total power consumption mean the sum during both static and dynamic operations.



ig. 8 Power Dissipation per gate - Input Frequency

#### 3.4 Static power consumption

There are no drain currents because one input transistor is always OFF when the input voltages of CMOS logic IC are lower than the threshold voltage  $(V_T)$  of a N-channel transistor or higher than the difference between the supply voltage and the threshold voltage  $(V_{DD}-V_T)$  of a P-channel transistor. The drain currents flow because the N-channel transistor is ON when the input voltage is about the threshold voltage  $(1.5V \ typ.)$  of an N-channel transistor.

Fig. 9 shows the drain currents as a function of CMOS logic input voltage. The drain currents reach maximum value at  $1/2~V_{DD}$ , and peak depends upon the squareness of the transistor use. The currents increase in proportion to  $V_{DD}^{\ n}$  if n>2.

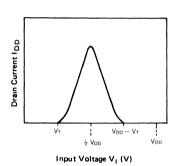


Fig. 9 Drain Current - Input Voltage

#### 3.5 Propagation Delay Time (Transfer Time)

Compared to the TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading (Fig. 10).

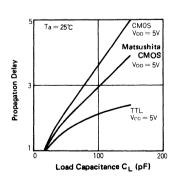


Fig. 10 Propagation Delay — Loading Capacitance Fig. 12 (TTL, Other CMOS, Matsushita CMOS)

The MN4000B series use both Matsushita's original Processing and improved circuit design to achieve propagation delays and output rise time that are superior to any other junction-isolated CMOS device.

Matsushita's original processing achieves lower parastic capacitances, which reduce the on-chip delay and increase the maximum clock frequency of flipflops, registers and counters. Buffering all outputs even on gates results in lower output impedance and thus reduces the effect of capacitive loading.

You should pay attention to design the system that the speed is important since propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

#### 3.6 Capacitive Loading Effect

A TTL with an output impedance  $25\Omega$  typ. in the low state is little affected by an increase in capacitive loading. A CMOS, however, with an output impedance of  $250\Omega$  typ. (5V operation), is 10 times more sensitive to capacitive loading. Fig. 11 shows the propagation delay time of the MN4011B as a function of load capacitance. Fig. 12 also shows the positive and negative-going delays as a function of load capacitance. It is limited in detail in general and individual specifications. The output with unbuffered gates has a higher output impedance and is more sensitive to capacitive loading.

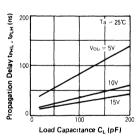
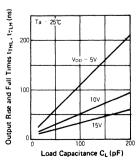


Fig. 11 Propagation Delay - Loading Capacitance



Output Rise and Fall Times — Loading Capacitance (output transient times)

#### 3.7 Supply Voltage Effect

#### 3.7.1 Speed

Fig. 13 shows propagation delay as a function of supply voltage. The best choice for slow applications is 5V. For reasonably fast systems, choose 10 or 12V. Any application requiring 15V to achieve less delays and fast operation should be weighed against an LS-TTL approach.

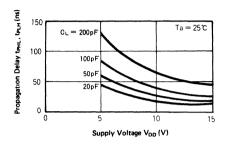


Fig. 13 Propagation Delay Versus Supply Voltage of MN4011B

#### 3.7.2 Noise Immunity

The noise immunity is improved according to the increase of supply voltage.

#### 3.8 Temperature Effect

The temperature dependence of the CMOS is much less than for the TTL. For the TTL there are three factors: increase of  $\beta$  with temperature, increase of resistor value with temperature and decrease of junction forward voltage drop with increasing temperature. For the CMOS, essentially only the carrier mobility changes, thus increasing the impedance and the delay with temperature. Please refer to the common and individual specifications in detail.

Fig. 14 shows propagation delay of the MN4011B as a function of ambient temperature.

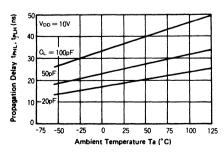


Fig. 14 Propagation Delay Versus Ambient Temperature at V<sub>DD</sub> = 10V of MN4011B

#### 3.9 Noise immunity

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, the CMOS can claim very good voltage noise immunity. Its typical values are 2.25V in a 5V system, 4.5V in a 10V system and 6.75V in a 15V system.

Fig. 15 shows the transfer comparison with the TTL. This implies the 1V noise immunity in a lightly loaded system and only 0.4V in the worst case. Fig. 16 shows the transfer characteristics at ambient temperatures ranging from  $-55^{\circ}$ C to  $+125^{\circ}$ C.

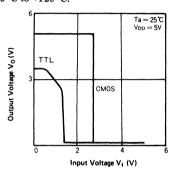


Fig. 15 Standard Transfer Characteristics of TTL and CMOS

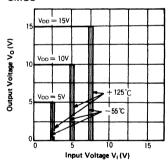


Fig. 16 Voltage Transfer Characteristics at  $Ta = -55^{\circ}C$ .

Since the CMOS output impedance, output voltage and input threshold voltage are symmetrical with respect to the supply voltage, the Low and High level noise immunity are practically equal. Therefore, a CMOS system can tolerate ground or  $V_{\rm DD}$  drops and noise on these supply lines of more than 1V, even in a 5V system. Moreover, the inherent CMOS delays act as a noise filter; 10ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, the CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.



The output impedance of the CMOS is 3 to 10 times higher than that of the TTL. CMOS interconnections are less stiff and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, Table 2 shows a comparison of the CMOS with the TTL. It is apparent that the dynamic noise immunity of the CMOS at 10V operation is almost equal to the TTL and is 3 times higher than that of the LS-TTL.

The CMOS is less affected by noise immunity due to ideal transfer characteristics and comparatively slow speeds, but the TTL/LS-TTL is 5 times more sensitive to noise immunity than the CMOS.

Table 2 Dynamic Noise Immunity for CMOS, TTL and

$V_{DD}$	5 V	10V	15V
CMOS/TTL	0.5	1	2
CMOS/LS-TTL	1	3	5

#### 3.10 Input Protection

The gate input to any MOS transistor appears like a small (< 1pF) very low leakage (<  $10^{-12}$  A) capacitor which is isolated from the substrate by an about 1000A thick  $SiO_2$ . Without special precautions, these inputs could be electrically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

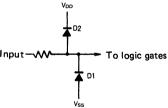


Fig. 17 Standard Input Protection Circuit of MN4000B series

Except for some devices, the MN4000B series utilize a series resistor, nominally 400 to  $500\Omega$ , and two diodes, one to  $V_{DD}$ , and another to  $V_{SS}$ . The resistor is a polysilicon true resistor without a parasitic substrate diode. This ensures that the input impedance is always over  $400\Omega$  under all biasing conditions. The diode  $(D_1)$  is connected to  $V_{SS}$  in parallel, and exhibits typical forward voltage drops of 0.9V at 1mA and reverse breakdown of 20V. For certain special applications such as

oscillators, the diodes actually conduct during normal operation. In this case, the input currents might be limited to under 1mA. Currents over 10mA might damage the device.

Fig. 18 shows the input protection circuit of the MN4049B and MN4050B. The diode  $(D_1)$  is a drain against  $V_{SS}$  of the protection device.

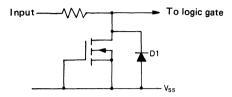


Fig. 18 Input Protection Circuit of MN4049B and MN4050B

#### 3.11 Power Supply Regulation and Decoupling

Since the CMOS has a wide operation range of 3V to 15V, it is considered that there is no need to regulate the power supply. However, the supply voltage strongly affects the system speed, noise immunity and power dissipation, so please refer to another text with respect to this value. There are some cases when voltage spikes generated by other systems override on the power line. These spikes affect noise immunity and damage the circuit at worst or adversely affect operation. It is necessary to connect a decoupling capacitance on the power line. A few  $\mu$ F of electrolytic capacitance per ten devices is generally adequate. But careful attention should be paid in special cases. cases.

- MN4511B: BCD-7 segment Latch/Decoder/Driver;
   Connecting 3μF electrolytic capacitance to each device, it is necessary to avoid abnormal voltage spikes due to high di/dt.
- MN4528B: Trigger/Resettable Dual Monostable multivibrator; an appropriate decoupling capacitance should be used for this kind of circuit.
- The supply voltage of min. 4V is required for the circuit of Liner operation like RC or Xtal oscillator.

#### 3.12 Tristate Output

In the case of the control input (EO) High, outputs are enabled and both  $P_4$  and  $N_4$  transistors function as a transmission gate, and connect two gates of output transistors. In the case of the control input (EO) Low, outputs are high impedance state (OFF) and  $P_3$  transistors are pull-up,  $N_3$  transistors pull-down respectively. (Refer to Fig. 19, Fig. 20)

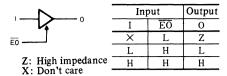


Fig. 19 Tristate Logic Symbol and Truth Table

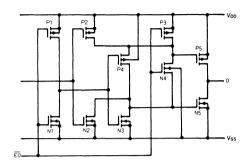


Fig. 20 Tristate Output Circuit

#### 3.13 Latch Up

There is a latch-up phenomenon in the CMOS as the specific problem. The latch-up is (thyristor) phenomenon which comes from the parastics PNP and NPN transistors which are physical contruction of CMOS though it does not occur within maximum rating. This phenomenon results in much current between  $V_{\rm DD} \sim V_{\rm SS}$  with ON state of parasitics thyristor because input or output currents abnormally reverse if there are unexpected surges exceeding maximum rating, ripples of power supply, noises and some differences of the rising time when the IC is operated by two power supplies. While this phenomenon is positive feedback, it cannot be avoided unless the power is turned off or the current is limited under an appropriate value.

If the latch-up occurs when the set is operating, it possively aires the set crucial damage after damaging the IC in the worst case.

It is accordingly necessary to give sufficient consideration to not causing the latch-up during set design. It is necessary to design so as not to cause a forward current through the input protection diode or output parasitic diode which become the trigger of latch-up when the input voltage is higher than  $V_{DD}$  or lower than  $V_{SS}$ . or lower than  $V_{SS}$ .

We intend to design so as not to cause the latch-up by considering the  $\beta$  of the parasitic transistor and the depth of a diffusion. We assure that there are no problems in normal usage, according to evaluations of the level which occurs the latch-up shown in Fig. 21.

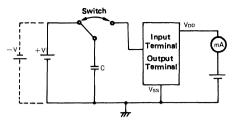


Fig. 21 Measurement of Latch-up

Let us explain in general how to protect against, the latch-up.

- A. Insert the capacitor (0.1 $\mu$  ~ 10 $\mu$ F) between V<sub>DD</sub> ~ V<sub>SS</sub>.
- B. Limit the charging current to less than 10mA inserting dumper registers into shunt diodes if the load capacitor is large, though it is desiable to be under 1000pF. (Fig. 22)
- C. It is recommended not to apply the input signal prior to V<sub>DD</sub>; otherwise insert dumper resistors to the input.
- D. Insert an appropiate value of resistors in series with to input in order to be under 10mA for the input current.

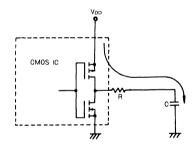


Fig. 22 Less Output Capacitance and Output Current Under 10mA

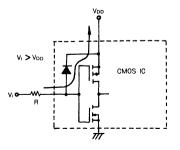


Fig. 23 If Input is Applied Earlier than Power Supply



#### 3.14 How to Terminate Unused Input

If the input is open, the output is unsteady due to indefinite input potential, because CMOS input impedance is very high. It is recommended that unused inputs be connected to  $V_{DD}$  in case of NAND gates or are to  $V_{SS}$  in case of NOR gates directly or through resistors ranging from  $10k\Omega$  to  $100k\Omega$ .

#### 3.15 Parallel Connection

The fan-outs can be increased by connecting in parallel with the same kind of gate. The switching speeds are improved by this means.

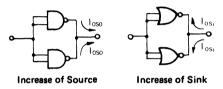


Fig. 24 Expansion of Fan-Out by Parallel Connection

#### 3.16 It is not recommended to used a wired OR.

Fig. 25 shows that the correct logic level cannot be obtained from the outputs of which voltage becomes about a half level ( $V_{\rm DD} \sim V_{\rm SS}$ ) because, when  $I_1 = I_2$  is Low and  $I_3 = I_4$  is High, the output voltage is determined by the ratio of P-channel and N-channel MOS transistors being ON.

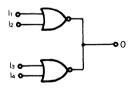


Fig. 25 Wired OR Connection (Inhibit)

#### 3.17 Output short

Do not short the outputs  $(V_{DD})$  or  $V_{SS}$  as there are no protection circuits that limit output currents. A long duration of output short may damage the device. Considering steady operation and reliability, it is advised that the maximum output currents should be within 1.5 times those at  $V_{DD}$  = 15V

#### 4. How to Handle The MOS Device

All our MOS IC devices contain circuitry to protect the input against damage due to high static voltages or electric fields; however care should be taken so avoid chance accidents.

#### 4.1 Human Body

The operators who test or handle the device should be careful to ground themselves through the registers (1  $\sim$  10M $\Omega$ ).

#### 4.2 Storing and Transportation

Store and transport the devices in the original cases which we offer. A conductive material or special magazine rail is suitable for use. These are used so all leads of ICs are shorted or isolated from external fields.

#### 4.3 Testing and Handling

The testing or transfer from the carrier to another place should be done on a conductive board (metall board, etc.). The operators should be grounded electrically to a conductive table (for instance, through metarllic cords or chains) while testing or handling. The earth terminals of instruments for testing or handling should be connected to the same table. Do not apply the signal while the device power is OFF.

#### 4.4 Attachment

To protect against defects in production, MOS ICs should be attached to the PC board after attaching all other parts and the ICs, metallic parts of the board, instruments and operators are connected to the same potential (earth). If earthing is not possible, operators should touch the PC board before attaching MOS ICs to it.

#### 4.5 Soldering

The tip of the soldering iron, including low voltage ones, and the solder pot should be kept at the same potential as the MOS IC and PC board.

#### 4.6 Static Electric Field

Operators should wear clothing which is unlikely to generate static electricity. (Wool, silk and synthetic fibers are unsuitable.) After attaching the MOS IC to the PC board, it is recommended that a conductive clip or tape should be connected to the PC board in order to protect against static electricity, because the PC board is a part of the leads from the IC until the appropriate voltage is applied to the completed PC board.

#### 4.7 Terminal Voltage

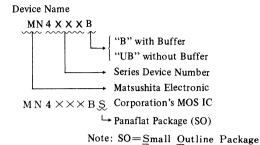
Do not insert or remove the PC board (including CMOS devices) with the power applied, in order to avoid permanent damage by excessive voltage.

#### 4.8 Surge Voltage

Surge voltage such as power ON-OFF, relay, etc. should be removed.

#### 5. Ordering and Marking

Matsushita CMOS devices may be ordered by using a simplified purchasing code.



#### Current

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

II	Input Current	The current flowing into a device at specified input voltage and VDD.
$I_{OH}$	Output High Current	The drive current flowing out of the device at specified High output voltage and $V_{\rm DD}$ .
$I_{OL}$	Output Low Current	The drive current flowing into the device at specified Low output voltage and V <sub>DD</sub> .
$I_{DD}$	Quiescent Power Supply Current	The current flowing into the $V_{DD}$ lead at specified input and $V_{DD}$ conditions.
$I_{OZ}$	Output OFF Current High	The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified High output voltage and V <sub>DD</sub> .
$I_{IL}$	Input Current Low	The current flowing into a device at a specified Low level input voltage and a specified $V_{\mbox{\scriptsize DD}}$ .
IIH	Input Current High	The current flowing into a device at a specified High level input voltage and a specified $V_{\mathrm{DD}}$ .
$I_{DDL}$	Quiescent Power Supply Current Low	The current flowing into the $V_{DD}$ lead with a specified Low level input voltage on all inputs and specified $V_{DD}$ conditions.
I <sub>DDH</sub>	Quiescent Power Supply Current	The current flowing into the $V_{DD}$ lead with a specified High level input voltage on all inputs and specified $V_{DD}$ conditions.

#### Voltages

All voltage are referenced to the VSS which is the most negative potential applied to the device.

$V_{DD}$	Drain Voltage	The most positive potential on the device.
$V_{SS}$	Source Voltage	For device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.
$V_{EE}$	Source Voltage	One of two negative power supplies, the most negative power supply used as a reference level for other voltages.
$V_{IH}$	Input High Voltage	The range of input voltages that represents a logic High level in the system.
$v_{IL}$	Input Low Voltage	The range of input voltages that represents a logic Low level in the system.
$v_{OH}$	Output High Voltage	The range of voltages at an output terminal with specified output loading and supply voltage.
$V_{OL}$	Output Low Voltage	The range of voltages at an output terminal with specified output loading and supply voltage.



#### **Explanation**

#### Analog Terms

R <sub>ON</sub>	ON Resistance	The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V <sub>DD</sub> .
ΔR <sub>ON</sub>	"Δ" ON Resistance	The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and $V_{\rm DD}$ .

#### • AC Switching • Parameters

$f_i$	Input Frequency	t <sub>w</sub>	Pull Width
$f_o$	Output Frequency	<sup>t</sup> hold	Hold Time
$f_{max}$	Maximum Clock Frequency	t <sub>su</sub>	Set-Up Time
tr, tf	Clock Input Rise, Fall Time	t <sub>PHZ</sub>	3-State Output Disable Time H → Z
tPLH	Transfer Delay (Propagation Delay Time)	tPLZ	3-State Output Disable Time L → Z
<sup>t</sup> PHL	Transfer Delay (Propagation Delay Time)	t <sub>PZH</sub>	3-State Output Enable Time Z → "H"
t <sub>TLH</sub>	Rise Time L → H	tPZL	3-State Output Enable Time Z → "L"
t <sub>THL</sub>	Fall Time H → L	t <sub>R</sub>	Recovery Time

# General Specifications



#### **GENERAL SPECIFICATIONS CONTENTS**

1.	Absolute Maximum Ratings	2:
2.	Main Characteristics Figures	2:
3.	DC Characteristics	2
4.	Switching Characteristics	21
5.	Mechanical Data	,,

#### **MN4000B Series General Specifications**

The MN4000B series operate in the range that VDD is +3  $\sim$  +15V ( $V_{SS}$  = 0V) but all ratings are guaranteed at the 3 points of 5V, 10V and 15V. Because the CMOS logic has wide operation range as mentioned above, it is not so critical on source regulation as conventional logic ICs (TTL, LS-TTL, etc.) If speed, noise margin, interface to other systems, etc. are not a concern, it operates at  $V_{DD} = +3V$  (min). If power consumption and interface to other systems are not a concern, it operates at V<sub>DD</sub> = +15V (max.). Connect unused input terminals to VDD, VCC or other input terminals. Although treatment against static electricity is conducted on I/O terminals of CMOS logic ICs, precautions against static electricity during handling are recommended.

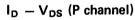
Ratings are described in individual data sheets. However, to assist understanding the outline of the MN4000B series' CMOS logic ICs, specifications which are common in general are shown hereunder.

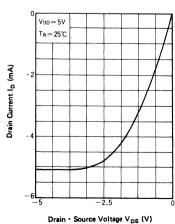
#### 1. Absolute Maximum Ratings (V<sub>SS</sub> = 0V)

	Iter	n	Symbol	Rating	Unit
Supply Voltage			$V_{ m DD}$	-0.5∼+18	V
Input Voltage			$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage			$v_{o}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input • Output Current		±Ι	max. 10	mA	
	MN4××××B	Ta=-40~+60°C	P <sub>D</sub> **	max. 400	mW
Power	(DIL Package)	Ta=+60~+85°C	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Dissipation	MN4XXXXBS	Ta=-40~+60℃	ח	max. 275	mW
	(Dil Package)	Ta=+60~+85°C	$P_D$	Decrease up to 200mW rating at 3.8mW/°C	mW
Power Dis	sipation (Per	output terminal)	$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage To	emperature		Tstg	-65~+150	C

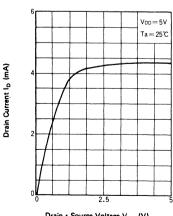
 $<sup>^*</sup>V_{DD} + 0.5V$  should be under 18V. \*\*Individual specifications are described in DIL package type.

#### 2. Main Characteristics Figures

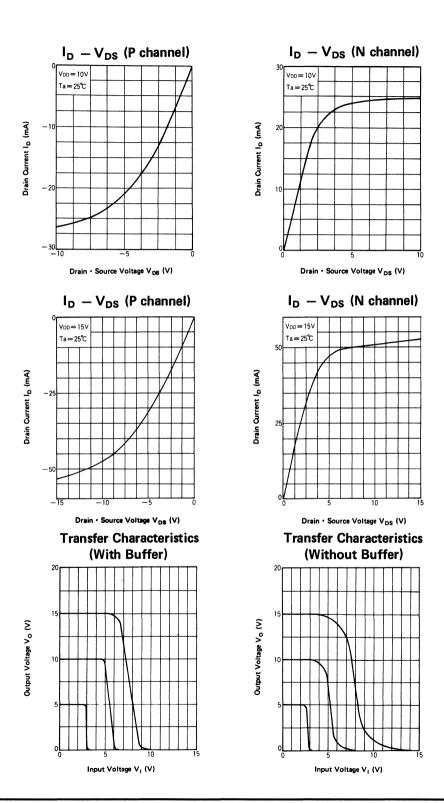




#### I<sub>D</sub> - V<sub>DS</sub> (N channel)



Drain · Source Voltage V<sub>DS</sub> (V)



# 3. DC Characteristics DC Characteristics (V<sub>SS</sub> = 0V; Implicit case)

	Item	$V_{\mathrm{DD}}$	Symbol	Conditions	Ta=-	-40℃	Ta=2	5℃	Ta=	<b>85</b> ℃	Unit
	710111	(V)	Dymoor	Conditions	min.	max.	min.	max.	min.	max.	
	cent Power										
Suppi	y Current	5			_	1		1	-	7.5	μA
Gat	es	10	$I_{DD}$			2		2		15	μA
		15	l			4	_	4		7.5	
		5		all valid input combinations,	_	4	_	4		30	μA
Buf	fers, flip-flops	10	$I_{ m DD}$	$V_{\rm I} = V_{\rm SS}$ or $V_{\rm DD}$		8	- 1	8	-	60	μA
		15		11 133 01 100		16		16	-	120	μA
		5				20		20	-		μA
MS	SI	10	$I_{DD}$			40		40		300	μA
		15		]		80		80			<u> </u>
Outn	st Voltage	5				0.05		0.05		0.05	
		10	Vol	$V_{\rm I} = V_{ m SS}$ or $V_{ m DD}$ , $ I_{ m O}  < 1 \mu { m A}$		0.05		0.05		0.05	
		15				0.05		0.05		0.05	
Outn	ut Woltogo	5			4.95		4.95		4.95	_	V
		10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $V_{\rm DD}$ , $ I_{\rm O}  < 1\mu$ A	9.95		9.95	_	9.95		
		15			14.95		14.95		14.95		
	Voltage	5		$V_0 = 0.5 V \text{ or } 4.5 V$	_	1.5	_	1.5		1.5	V
		10	$V_{IL}$	$V_0 = 1.0 \text{V or } 9.0 \text{V}    I_0   < 1 \mu \text{A}$	_	3	_	3	_	3	V
(OIII)		15		V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	<u> </u>
Input	Voltage	5		$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5	_	3.5		3.5	_	V
		10	$V_{IH}$	$V_0 = 1.0 \text{V or } 9.0 \text{V}  I_0  < 1 \mu \text{A}$	7		7	_	7.		V
(Omy	Tor Burrer)	15		V <sub>0</sub> =1.5V or 13.5V	11		11		11		
Input	Voltage	5		$V_0 = 0.5 V \text{ or } 4.5 V$		1		1	-	_	
		10	$V_{IL}$	$V_0 = 1.0 \text{V or } 9.0 \text{V}  I_0  < 1 \mu \text{A}$		2		2	_	2	V
(EXC	pt for Burier)	15		V <sub>0</sub> =1.5V or 13.5V		2.5		2.5		2.5	V
Input	Voltage	5	ł	$V_0 = 0.5 \text{V or } 4.5 \text{V}$	4	-	4	_	4		V
		10	$V_{IH}$	$V_0 = 1.0 \text{V or } 9.0 \text{V}  I_0  < 1 \mu \text{A}$	8	-	8		8		V
(LACC	pt for buffer)	15		V <sub>0</sub> =1.5V or 13.5V	12.5		12.5		12.5		V
Output Voltage Low Level  Output Voltage High Level  Input Voltage Low Level (Only for Buffer)  Input Voltage High Level (Only for Buffer)  Input Voltage Low Level (Except for Buffer)  Input Voltage Low Level (Except for Buffer)  Output (sink) Current Low Level  Output (source) Current High Level	5		$V_0 = 0.4V, V_I = 0 \text{ or } 5V$	0.52		0.44		0.36			
		10	$I_{OL}$	$V_0 = 0.5V, V_I = 0 \text{ or } 10V$	1.3	_	1.1	_	0.9	_	mA
		15		$V_0 = 1.5V, V_I = 0 \text{ or } 15V$	3.6		3		2.4		mA
Outni	it (cource)	5		$V_0 = 4.6V, V_I = 0 \text{ or } 5V$	0.52		0.44		0.36		mA
		10	$-I_{OH}$	$V_0 = 9.5V, V_1 = 0 \text{ or } 10V$	1.3		1.1	_	0.9	_	mA
		15		$V_0 = 13.5 \text{V}, V_I = 0 \text{ or } 15 \text{V}$	3.6		3	_	2.4		mA
Output (	Current High Level	5	$-I_{OH}$	$V_0 = 2.5V, V_I = 0 \text{ or } 5V$	1.7		1.4		1.1		mA
Input Le	akage Current	15	$\pm I_{\rm I}$	$V_{\rm I} = 0$ or $15$ V		0.3		0.3			<u> </u>
3-State Output Pin	Leakage Current High Level	15	I <sub>OZH</sub>	output returned to $V_{\mathrm{DD}}$		1.6	_	1.6			+
Output rift	Leakage Current Low Level	15	$-I_{OZL}$	output returned to V <sub>SS</sub>		1.6		1.6	<u></u>	12	μA



#### 4. Switching Characteristics

#### Clock Rise, Fall Times (t<sub>r</sub>, t<sub>f</sub>)

The upper limit of  $t_r$ ,  $t_f$  will depend on the device or supply voltage. Input clock rise and fall times are less than  $15\mu s$  at 5V operation, less than  $4\mu s$  at 10V operation, and less than  $1\mu s$  at 15V operation if not specified in individual data sheets.

#### Output Rise, Fall Time (t<sub>TLH</sub>, t<sub>THL</sub>)

 $V_{SS} = 0V$ , Ta = 25°C,  $C_L = 50$ pF, Input Rise • Fall Time  $\leq 20$ ns.

Item	$V_{DD} \ (V)$	Symbol	min.	typ.	max.		External Capacitance
Output Fall Time HIGH → LOW	5 10 15	t <sub>THL</sub>	_ _ _	60 30 20	120 60 40	ns ns ns	$\begin{aligned} &10 \text{ns} + (1.0 \text{ns/pF})  \text{C}_{\text{L}} \\ &9 \text{ns} + (0.42 \text{ns/pF})  \text{C}_{\text{L}} \\ &6 \text{ns} + (0.28 \text{ns/pF})  \text{C}_{\text{L}} \end{aligned}$
Output Rise Time LOW → HIGH	5 10 15	t <sub>TLH</sub>		60 30 20	120 60 50	ns ns ns	$\begin{aligned} &10 \text{ns} + (1.0 \text{ns/pF})  \text{C}_L \\ &9 \text{ns} + (0.42 \text{ns/pF})  \text{C}_L \\ &6 \text{ns} + (0.28 \text{ns/pF})  \text{C}_L \end{aligned}$

#### • Temperature Coefficient (Typical)

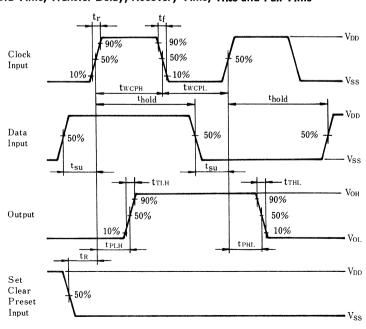
Transfer Delay (Propagation Delay Time) +0.35%/°C

Output Rise, Fall Time +0.35%/°C

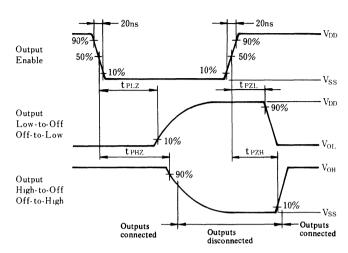
#### Input Capacitance (Digital Input)

Maximum Input Capacitance  $C_I = 7.5 pF$ 

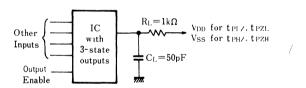
#### • Setup Time, Hold Time, Transfer Delay, Recovery Time, Rise and Fall Time



#### • Transfer Delay of Tristate Output

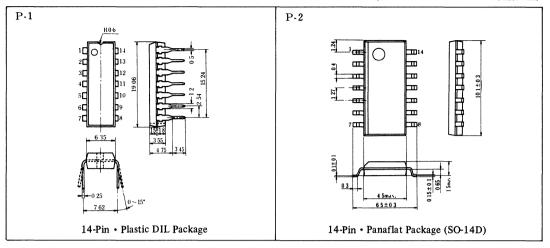


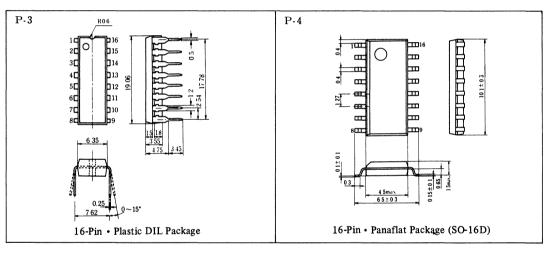
#### • Test Circuit of Tristate Output IC

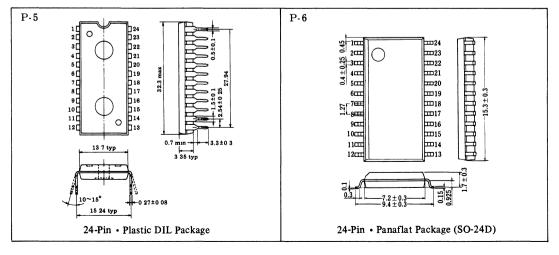


#### 5. Mechanical Data

Unit: mm







# **Individual Specifications**



#### **Index Table**

-								
	MN4000B/S	(33)	MN4027B/S	( 92)	MN4072B/S	(152)	MN4518B/S	(217)
	MN4001B/S	(35)	MN4028B/S	( 95)	MN4073B/S	(154)	MN4519B/S	(221)
	MN4002B/S	(37)	MN4029B/S	( 98)	MN4075B/S	(156)	MN4520B/S	(224)
	MN4006B/S	(39)	MN4030B/S	(103)	MN4076B/S	(158)	MN4526B/S	(228)
	MN4007UB/S	(42)	MN4035B/\$	(105)	MN4078B/S	(162)	MN4528B/S	(232)
	MN4008B/S	(44)	MN4040B/S	(109)	MN4081B/S	(165)	MN4531B/S	(236)
	MN4011B/S	(47)	MN4042B/S	(112)	MN4082B/S	(167)	MN4538B/S	(239)
	MN4012B/S	(49)	MN4043B/S	(115)	MN4085B/S	(169)	MN4539B/S	(243)
	MN4013B/S	(51)	MN4044B/S	(118)	MN4086B/S	(172)	MN4541B/S	(246)
	MN4015B/S	(54)	MN4046B/S	(121)	MN4093B/S	(175)	MN4543B/S	(249)
	MN4016B/S	(57)	MN4049B/S	(125)	MN4094B/S	(178)	MN4556B/\$	(253)
	MN4017B/S	(61)	MN4050B/S	(128)	MN4502B/S	(182)	MN4584B/\$	(256)
	MN4018B/S	(66)	MN4051B/S	(131)	MN4503B/S	(185)	MN4585B/S	(259)
	MN4019B/S	(70)	MN4052B/S	(135)	MN4510B/S	(188)	MN4724B/S	(262)
	MN4020B/S	(73)	MN4053B/S	(139)	MN4511B/S	(193)	MN40098B/S	(265)
	MN4021B/S	(77)	MN4066B/\$	(143)	MN4512B/S	(198)	MN40160B/S	(268)
	MN4022B/S	(80)	MN4068B/S	(146)	MN4514B/S	(202)	MN40161B/S	(272)
	MN4023B/S	(85)	MN4069UB/S	(148)	MN4515B/S	(205)	MN40174B/S	(277)
	MN4024B/S	(87)	MN4070B/S	(103)	MN4516B/S	(208)	MN40175B/S	(280)
	MN4025B/S	(90)	MN4071B/S	(150)	MN4517B/S	(214)		
_	<del></del>		L		L		L	

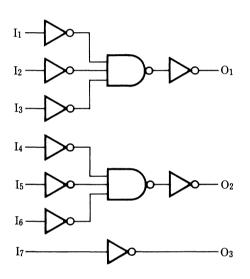
# MN4000B/MN4000BS

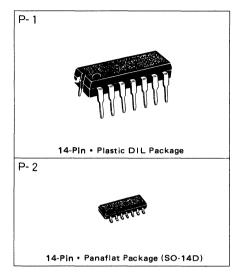
#### Dual 3-Input NOR Gates and Inverters

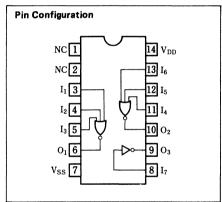
#### Description

The MN4000B/S are dual 3-input NOR gate and inverters. Their primary use is where low power dissipation and/or high noise immunity is desired.

#### Logic Diagram







#### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatu	re	Tstg	<b>−65~+150</b>	°C

<sup>\*</sup>  $V_{DD}$  + 0.5V should be under 18V



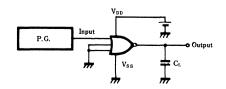
## $\blacksquare$ DC Characteristics $(V_{SS} {=} 0V)$

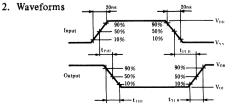
Item	$V_{DD}$	Sym-		1 4:4:	Ta=-	- <b>40</b> ℃	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	Unit
	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
	5				-	1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{DD}$		2		2	_	15	μA
	15				_	4	_	4	_	30	
_	5		37 – 37	V	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	$V_{ m DD}$	_	0.05		0.05		0.05	V
20.0.20.01	15		$ I_0  < 1\mu A$		_	0.05	_	0.05	_	0.05	
	5		37 — 37	37	4.95	_	4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I}=V_{\rm SS}$ or	V DD	9.95		9.95		9.95		V
	15		$ I_0  < 1\mu A$		14.95	_	14.95	_	14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3		3	v
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4	—	4	
* . ** 1.	5			Vo=0.5V or 4.5V	3.5	_	3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11		11		
_	5		$V_0 = 0.4V$	V <sub>I</sub> =0V or 5V	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I$ =0 $V$ or 10 $V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5V$ ,	$V_I$ =0 V or 15V	3.6	_	3		2.4		
	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0V or 5V	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 $V$ or $10V$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	$V_{\rm I} = 0  {\rm V}  {\rm or}  15  {\rm V}$	3.6		3		2.4		
Output Current High Level	5	—Іон	$V_0 = 2.5 V$	$V_I$ =0 $V$ or 5 $V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0V$ or	15V	_	0.3		0.3	_	1	μA

## Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5	,	_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
-	15		_	20	60	
Propagation Delay Time	5		_	70	210	
	10	t <sub>PHL</sub>	_	35	105	ns
$I_1 \sim I_6 \rightarrow O_1$ , $O_2$	15	t <sub>PLH</sub>	_	30	90	
Propagation Delay Time	5	_		45	135	
	10	t <sub>PHL</sub>	_	25	75	ns
I <sub>7</sub> →O <sub>3</sub>	15	t <sub>PLH</sub>	_	20	60	
Input Capacitance		Cı	_	<del>-</del>	7.5	pF

## 1. Switching Time Test Circuit





# MN4001B/MN4001BS

## Quad 2-Input NOR Gates

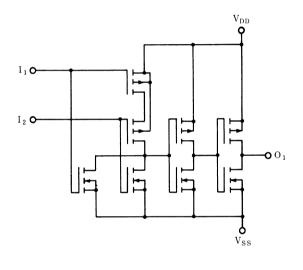
## Description

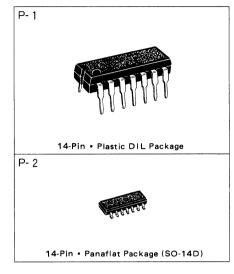
The MN4001B/S are positive 2-input NOR gates and have 4 circuits in a package.

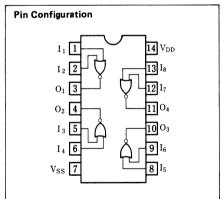
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time.

The MN4001B/S are equivalent to MOTOROLA MC14001B and RCA CD4001B.

## Schematic Diagram (1/4)







## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	${\mathbb C}$
Storage Temperature		Tstg	<del>-65</del> ∼+150	°C

**— 35 —** 



<sup>\*</sup> VDD + 0.5V should be under 18V

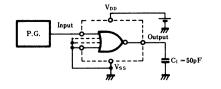
## $\blacksquare$ DC Characteristics $(V_{\rm SS}\!=\!0V)$

T4	$V_{DD}$	Sym-			Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	TT14
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
	5					1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		2		2	_	15	μA
	15					4		4		30	
	5		$V_i = V_{SS}$ or	V		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	V <sub>DD</sub>		0.05		0.05		0.05	V
20 11 20 101	15		10  < 1µA			0.05		0.05		0.05	
	5		$V_I = V_{SS}$ or	V	4.95	******	4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	V DD	9.95		9.95		9.95		V
	15		10  < 1µA		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Y-14	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7	********	7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0=0.4V$	$V_l = 0 V \text{ or } 5V$	0.52		0.44		0.36	_	
Output Current Low Level	10	IoL	$V_0=0.5V$	$V_I = 0 V \text{ or } 10V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	V <sub>1</sub> =0 V or 15V	3.6		3		2.4		
0 0	5		$V_0 = 4.6 V$ ,	$V_I = 0 V \text{ or } 5 V$	0.52	_	0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_l = 0  V \text{ or } 10  V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0V or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	$V_l = 0 V \text{ or } 5 V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_l = 0V$ or	15V		0.3		0.3		1	μA

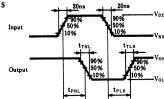
## 

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5		_	50	150	
Propagation Delay Time	10	t <sub>PLH</sub>		25	75	ns
	15		_	20	60	
	5			60	180	
Propagation Delay Time	10	t <sub>PHL</sub>	_	25	75	ns
	15			20	60	
Input Capacitance		Ci	_		7.5	pF

1. Switching Time Test Circuit



2. Waveforms



# MN4002B/MN4002BS

## Dual 4-Input NOR Gates

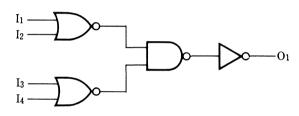
## Description

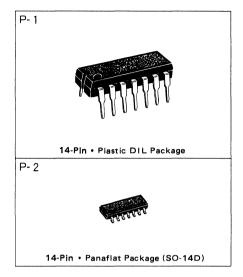
The MN4002B/S are positive 4-input NOR gates and have 2 circuits in a package.

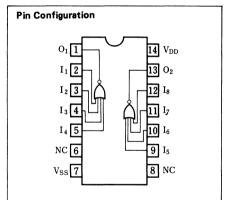
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4002B/S are equivalent to MOTOROLA MC14002B and RCA CD4002B.

## Logic Diagram (1/2)







## **Maximum Ratings** $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D.	max. 400	317
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	<del>-65</del> ∼+150	c

<sup>\*</sup> VDD + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

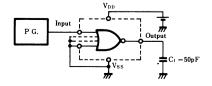
Item	$V_{DD}$	Sym-	,	Conditions	Ta=-	- <b>40</b> ℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0 : 4 %	5				_	1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2	_	2	_	15	μA
	15				_	4	_	4	_	30	
	5		37 — 37	37	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	$V_{ m DD}$	-	0.05		0.05	_	0.05	V
LOW LCVCI	15		$ I_0  < 1\mu A$		_	0.05		0.05	_	0.05	
	5		37 — 37	37	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	VoH	$V_I = V_{SS}$ or	V DD	9.95	_	9.95	_	9.95	-	V
mgn Lover	15		$ I_0  < 1\mu A$		14.95	_	14.95		14.95	_	
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3		3	V
Low Level	15			Vo=1.5V or 13.5V	_	4	-	4		4	
	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11	_	
	5		$V_0 = 0.4 V$	V <sub>l</sub> =0 V or 5V	0.52	_	0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_l = 0 V \text{ or } 10V$	1.3		1.1	_	0.9		mA
Low Level	15		$V_0 = 1.5V$ ,	$V_I = 0  \mathrm{V}  \mathrm{or}  15 \mathrm{V}$	3.6		3	_	2.4	_	
	5		$V_0 = 4.6V$	V <sub>i</sub> =0V or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$	$V_l = 0 V \text{ or } 10 V$	1.3		1.1	-	0.9		mA
111911 20.01	15		$V_0 = 13.5 V$	$V_{I} = 0 \text{ V or } 15 \text{ V}$	3.6		3	_	2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>1</sub> =0V or 5V	1.7	_	1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0V$ or	15V		0.3		0.3	_	1	μA

## 

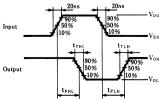
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
	5			50	150	
Propagation Delay Time	10	t <sub>PLH</sub>		25	75	ns
	15		_	20	60	
	5			60	180	
Propagation Delay Time	10	t <sub>PHL</sub>	_	25	75	ns
	15		_	20	60	
Input Capacitance		Cı		_	7.5	pF

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## 1. Switching Time Test Circuit







# MN4006B/MN4006BS

## 18-Bit Static Shift Registers

## Description

The MN4006B/S are maximum 18-bit static shift registers composed of two 4-bit shift registers and five 5-bit shift registers. Clock pulses for all registers are input through the common CP. By properly combining input and output, shift registers with the arbitrary stages of 4, 5, 8, 9, 10, 12, 13, 14, 16 and 17 are enabled.

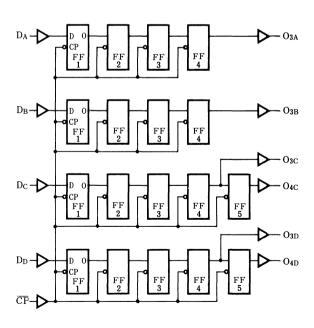
The MN4006B/S are equivalent to MOTOROLA MC14006B and RCA CD4006B.

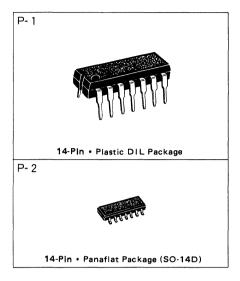
## Truth Table

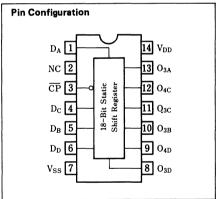
$D_n$	CP	$O_{n+1}$
$D_1$	_	$D_1$
×	\	no change

Note) X: don't care

## ■ Logic Diagram









## ■ Maximum Ratings (Ta=25°C)

Iter	n	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	<b>-0.5∼+18</b>	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	Current	$\pm I_I$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (p	per output terminal)	$P_D$	max, 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperature		Tstg	<b>−65~+150</b>	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

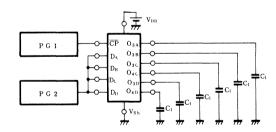
## $\blacksquare$ DC Characteristics $(V_{SS}{=}0V)$

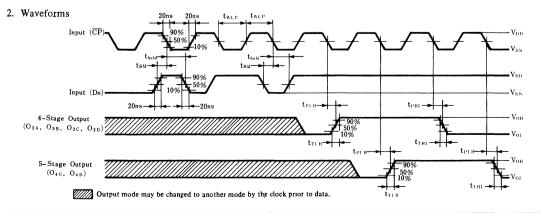
Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	T.T *4
item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0	5				_	20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40	_	40	_	300	μA
	15					80		80		600	
_	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol		V <sub>DD</sub>	_	0.05		0.05		0.05	V
2011 20101	15		$ I_0  < 1\mu A$			0.05		0.05	_	0.05	
	5		37 37	3.7	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	$V_{ m DD}$	9.95	_	9.95		9.95	-	V
<b>5</b> =	15		$ I_0  < 1\mu A$		14.95		14.95		14.95		
_	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3	_	3	_	3	V
20.1. 20.01	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
_	5			Vo=0.5V or 4.5V	3.5	_	3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
0	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4 V$	V <sub>i</sub> =0V or 5V	0.52	_	0.44		0.36		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I = 0 V \text{ or } 10 V$	1.3		1.1		0.9		mA
Low Lover	15		$V_0 = 1.5 V$ ,	$V_I$ =0 $V$ or 15 $V$	3.6		3		2.4		
_	5		$V_0 = 4.6 V$	V <sub>I</sub> =0V or 5V	0.52	_	0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$	$V_l = 0 V \text{ or } 10 V$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5V$	, $V_I = 0 V$ or $15 V$	3.6	_	3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>I</sub> =0V or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0V$ or	15V		0.3	-	0.3		1	μA

## $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	90	270	
Tropagation Delay Time  TP→On(H→L)	10	t <sub>PHL</sub>	_	40	120	ns
CP→On(H→L)	15		_	30	90	
Propagation Delay Time	5		_	90	270	
	10	t <sub>PLH</sub>	_	40	120	ns
$\overline{\mathbb{CP}} \rightarrow \operatorname{On}(L \rightarrow H)$	15		_	35	105	
	5		_	30	90	
Minimum Clock Pulse Width	10	twcph	_	20	60	ns
	15		_	15	45	
Set-up Time	5		_	10	30	
Dn→ <del>CP</del>	10	tsu	_	5	15	ns
Dn→CP	15			0	10	
Hold Time	5			-5	10	
Dn→ <del>CP</del>	10	thold		0	10	ns
Dn→Cr	15		_	0	10	
	5		9	18	_	
Maximum Clock Frequency	10	fmax	15	30	_	MHz
	15		18	36	_	
Input Capacitance		C <sub>I</sub>	_	_	7.5	pF

## 1. Switching Time Test Circuit







# MN4007UB/MN4007UBS

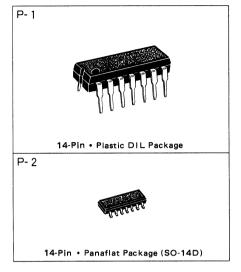
## Dual Complementary Pairs and Inverters

## Description

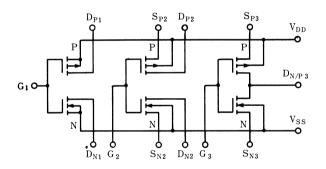
The MN4008UB/S are inverters in which a pair of the same 3-element N channel enhancement MOS FETs as 3-element P channel enhancement MOS FETs are incorporated in a package. One pair is the inverter and the other two are the complementary pair; source and drain are differently output.

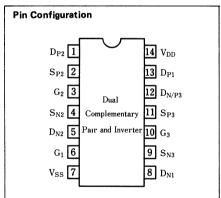
The MN4007UB/S have been widely applied to inverters, pulse-shaping circuits, NAND (NOR) gates, linear amplifiers, clock gates, transmission gates, high fan-out buffers, etc.

The MN4007UB/S are equivalent to RCA CD4007UB.



## Segment Configuration





## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (1	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	e e	Tstg	<b>−65~+150</b>	$^{\circ}$

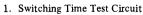
<sup>\*</sup> VDD + 0.5V should be under 18V

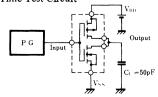
## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

74	$V_{ m DD}$	Sym-		N 4:4:	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	85℃	Unit
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
	5					1		1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2	_	2		15	μA
Supply Carrons	15						-	4	_	30	
	5		37 37	$V_1 = V_{SS}$ or $V_{DD}$			_	0.05	_	0.05	
Output Voltage Low Level	10	Vol		$V_{\mathrm{DD}}$	_	0.05	_	0.05	_	0.05	V
Low Level	15		$ I_{\rm O}  < 1\mu A$			0.05	_	0.05	_	0.05	
	5		37 37	17	4.95	_	4.95		4.95	_	
Output Voltage High Level	10	Voh	$V_I = V_{SS}$ or	V <sub>DD</sub>	9.95		9.95	_	9.95		V
	15		$ I_{\rm O}  < 1\mu A$		14.95	_	14.95		14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V		3	_	3		3	V
Low Level	15			V <sub>0</sub> =1.5V or 13.5V	_	4	_	4	_	4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11	_	11	_	
	5		$V_0 = 0.4 V$	V <sub>l</sub> =0 V or 5V	0.52		0.44	_	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_l = 0 V \text{ or } 10 V$	1.3		1.1		0.9		mA
Low Level	15		$V_0 = 1.5 V$	$V_l = 0 V \text{ or } 15V$	3.6	_	3		2.4		
	5		$V_0 = 4.6 V$	V <sub>I</sub> =0V or 5V	0.52	_	0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$	$V_I = 0 V \text{ or } 10 V$	1.3		1.1		0.9	-	mA
	15		$V_0 = 13.5 V$	$V_{I} = 0 V \text{ or } 15 V$	3.6	_	3	_	2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0V or 5V	1.7	_	1.4		1.1	_	mA
Input Leakage Current	15	±Ιι	V <sub>l</sub> =0V or	15 V		0.3	_	0.3		1	μA

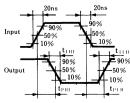
## 

Item	$V_{\mathrm{DD}}\left(\mathrm{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		-	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Decreasion Dalay Time	5		_	40	120	
Propagation Delay Time	10	t <sub>PHL</sub>	_	20	60	ns
$Gn-D_N; D_P (H \rightarrow L)$	15		_	15	45	
Proposition Deley Time	5			40	120	
Propagation Delay Time	10	t <sub>PLH</sub>		20	60	ns
$Gn-D_N; D_P (L\rightarrow H)$	15			15	45	
Input Capacitance		Cı	_		7.5	pF









# MN4008B/MN4008BS

## 4-Bit Full Adders

## Description

The MN4008B/S are 4-bit parallel processing full adders with a high-speed parallel carry circuit.

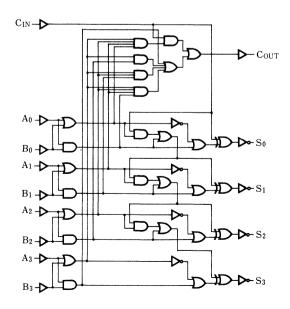
Summation of 4 added data input  $(A_0 \sim A_3)$ , another 4 adding data inputs  $(B_0 \sim B_3)$  and binary input added to carry input  $(C_{IN})$  from low row can be obtained by the binary code which is same as adding data outputs  $(S_0 \sim S_3)$  and carry output  $(C_{OUT})$ .

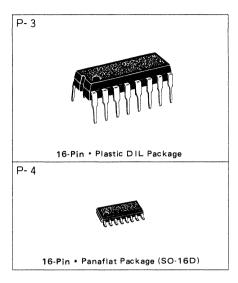
4 X n-bit addition by cascade connection and addition and subtraction circuit by external circuit can easily be composed.

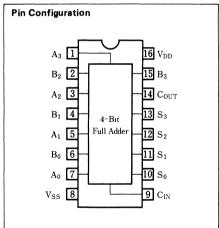
## Truth Table

	Input		Out	Output				
Cin	A	В	Соит	S				
L	L	L	L	L				
L	L	Н	L	Н				
L	Н	L	L	Н				
L	Н	Н	Н	L				
Н	L	L	L	Н				
Н	L	Н	Н	Ļ				
Н	Н	L	Н	L				
Н	Н	Н	Н	Н				

## Logic Diagram







## $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	mW
(per package)	Ta=+60~+85℃	$P^{D}$	Decrease up to 200mW rating at 8mW/°C	m vv
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	$^{\circ}$
Storage Temperatur	re	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

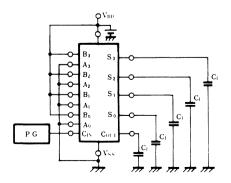
Item	$V_{\mathrm{DD}}$	Sym-	(	Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	mın.	max.	Unit
	5				_	20		20	-	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40	_	40		300	μA
Supply Culton	15					80	_	80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	_	0.05		0.05		0.05	V
	15		$ 1_0  \leq 1 \mu A$		_	0.05		0.05		0.05	
	5		V <sub>I</sub> =V <sub>SS</sub> or	17	4.95	_	4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1 \mu A$	$\mathbf{v}_{\mathrm{DD}}$	9.95		9.95		9.95	_	V
	15		$ 10  < 1 \mu A$		14.95		14.95		14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3		3	V
	15			Vo=1.5V or 13.5V		4	_	4	Washer .	4	
Immed Walters	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	-	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11		11		
	5		$V_0 = 0.4 V$ ,	$V_i = 0 V \text{ or } 5V$	0.52	_	0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_l = 0 V \text{ or } 10 V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_i = 0 V \text{ or } 15V$	3.6	_	3	*********	2.4	Variation	
0 0	5		$V_0 = 4.6 V$	$V_l = 0 V \text{ or } 5 V$	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_l = 0  \mathrm{V}  \mathrm{or}  10 \mathrm{V}$	1.3		1.1	_	0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>1</sub> =0V or 15V	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>i</sub> =0V or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>i</sub> =0V or	15V		0.3		0.3		1	μA



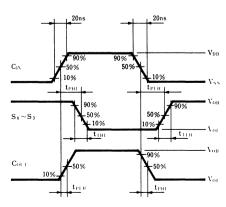
## $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_{L}\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time	10	t <sub>THI</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	135	405	
	10	tPLH		55	165	ns
Sum in $\rightarrow$ Sum out (L $\rightarrow$ H)	15		_	40	120	
Propagation Delay Time	5		_	150	450	
Sum in→Sum out (H→L)	10	t <sub>PHI</sub>		55	165	ns
Sum in→Sum out (H→L)	15		_	40	120	
Propagation Delay Time	5			100	300	
• •	10	$t_{\rm PLH}$	_	45	135	ns
$Sum n \rightarrow Cout (L \rightarrow H)$	15			30	90	
Propagation Delay Time	5		_	125	375	
Sum in→Cout (H→L)	10	t <sub>PHI</sub>	_	50	150	ns
Sum in→Cout (H→L)	15		_	35	105	
Danasaskia a Dalas Tima	5			115	345	
Propagation Delay Time	10	$t_{PLH}$	_	50	150	ns
$C_{I \setminus} \rightarrow Sum \ out (L \rightarrow H)$	15		_	35	105	
Propagation Delay Time	5			130	390	
$C_{IN} \rightarrow Sum out (H \rightarrow L)$	10	t <sub>PHL</sub>		50	150	ns
CN→Sum out(H→L)	15		-	35	105	
Propagation Delay Time	5		_	75	225	
• -	10	t <sub>PLH</sub>	_	35	105	ns
$C_{1} \rightarrow Cout(L \rightarrow H)$	15		_	25	75	
Propagation Delay Time	5		_	90	270	
	10	t <sub>PHL</sub>	_	35	105	ns
$C_{IN} \rightarrow Cout (H \rightarrow L)$	15		_	25	75	
Input Capacitance		Cı	_	_	7.5	pF

## 1. Switching Time Test Circuit



## 2. Waveforms



# MN4011B/MN4011BS

## Quad 2-Input NAND Gates

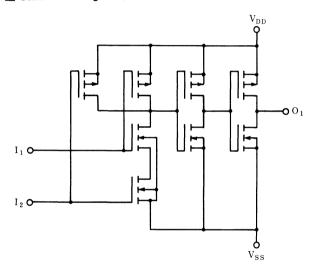
## Description

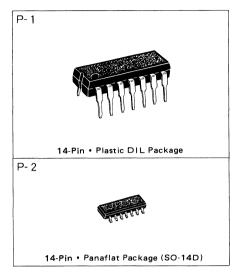
The MN4011B/S are positive 2-input NAND gates and have 4 circuits in a package.

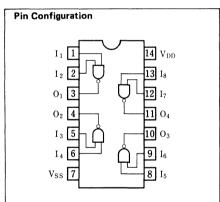
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4011B/S are equivalent to MOTOROLA MC14011B and RCA CD4011B.

## Schematic Diagram (1/4)







## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{DD}$	-0.5~+18	V	
Input Voltage		VI	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	] mvv	
Power Dissipation (per output terminal)		P <sub>D</sub>	max. 100	mW	
Operating Ambient Temperature		Topr	<b>−40~+85</b>	$^{\circ}$ C	
Storage Temperatu	re	Tstg	<del>-65~+150</del>	°C	

<sup>\*</sup>  $V_{DD}$  + 0.5V should be under 18V



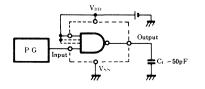
## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{ m DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	Unit
item	(V)	bol	`	Conditions		max.	min.	max.	min.	max.	Unit
	5					1		1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I}=V_{SS}$ or	$V_{DD}$		2		2		15	μA
	15					4		4	_	30	
_	5		V-V	37		0.05		0.05	Military.	0.05	
Output Voltage Low Level	10	$V_{OL}$	$V_I = V_{SS}$ or	$V_{ m DD}$	_	0.05	_	0.05		0.05	V
Low Level	15		$ I_{\rm O}  < 1\mu A$			0.05		0.05		0.05	
0	5		V V	17	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	V DD	9.95		9.95		9.95		V
	15		$ I_{\rm O}  < 1\mu A$		14.95		14.95		14.95		
	5		$ I_0  < 1\mu A$	V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$		Vo=1V or 9V		3		3		3	V
Eow Eurer	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4	_	4	
	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11	NATIONAL PROPERTY.	11		
	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 V or 5V	0.52		0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_i = 0 V \text{ or } 10V$	1.3		1.1		0.9		mA
Low Level	15		$V_0 = 1.5 V$ ,	$V_I = 0 V \text{ or } 15 V$	3.6		3		2.4		
	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0V or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$	$V_I = 0 V \text{ or } 10 V$	1.3		1.1	_	0.9	_	mA
ing. Leve.	15		$V_0 = 13.5 V$	, $V_l = 0 V$ or $15 V$	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>1</sub> =0V or 5V	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_l = 0V$ or	15V		0.3		0.3		1	μA

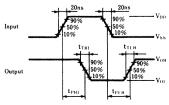
## ■ Switching Characteristics $(Ta=25^{\circ}C, V_{SS}=0V, C_L=50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub> ,		30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5		_	55	165	
Propagation Delay Time	10	t <sub>PI H</sub>		25	75	ns
	15		Marine Marine	20	60	
	5			55	165	
Propagation Delay Time	10	tPHL	_	25	75	ns
	15		_	20	60	
Input Capacitance		Cı	_	_	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



# MN4012B/MN4012BS

## Dual 4-Input NAND Gates

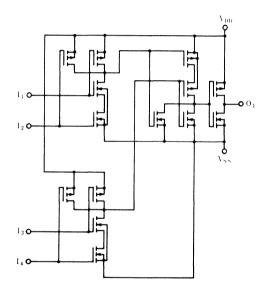
## Description

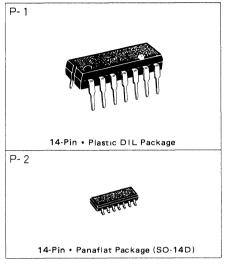
The MN4012B/S are positive 4-input NAND gates and have 2 circuits in a package.

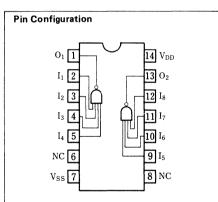
The outputs are fully buffered to improve propagation characteristics between the input and output which are affected by increasing of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4012B/S are equivalent to MOTOROLA MC14012B and RCA CD4012B.

## Schematic Diagram (1/2)







## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	mW
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	m vv
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

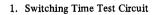


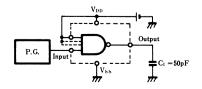
## $\blacksquare$ DC Characteristics $(V_{\rm SS}\!=\!0V)$

T4	$V_{\mathrm{DD}}$	Sym-		Sanditiana	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	I Imia
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
	5					1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		2	_	2		15	μA
	15					<b>4</b> <sup>-</sup>	_	4	_	30	
	5		$V_I = V_{SS}$ or	V	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	V <sub>DD</sub>	_	0.05		0.05	_	0.05	V
	15		$ 1_0  < 1\mu A$			0.05	_	0.05		0.05	
	5		$V_I = V_{SS}$ or	17	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	V DD	9.95	_	9.95	_	9.95	_	V
	15		10  < 1µA		14.95	_	14.95	_	14.95	_	
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
T 37 . 14	5			Vo=0.5V or 4.5V	3.5		3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
0	5		$V_0 = 0.4 V$ ,	$V_I = 0 V \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I = 0 V \text{ or } 10V$	1.3		1.1		0.9	_	mA
	15		$V_0 = 1.5 V$	$V_I = 0 \text{ V or } 15 \text{ V}$	3.6		3		2.4		
	5		$V_0 = 4.6 V$	$V_1 = 0 V \text{ or } 5 V$	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$	$V_I = 0 V \text{ or } 10 V$	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 13.5 \text{ V}$	, V <sub>1</sub> =0V or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	V <sub>i</sub> =0V or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_I$	$V_l = 0V$ or	15V		0.3		0.3	_	1	μΑ

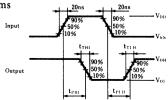
## 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
Output Fall Time	5		-	60	180	
	10	t <sub>THL</sub>	_	30	90	ns
	15		******	20	60	
	5			70	210	ns
Propagation Delay Time	10	t <sub>PLH</sub>		30	90	
	15			25	75	
	5			70	210	
Propagation Delay Time	10	t <sub>PHL</sub>	_	25	75	ns
	15		_	20	60	
Input Capacitance		Cı	_	_	7.5	pF









# MN4013B/MN4013BS

## Dual D-Type Flip-Flops

## Description

The MN4013B/S are dual D flip-flop. Each flip-flop has independent data, set, clear and clock inputs and complementary outputs  $(0,\overline{0})$  only on the positive going edge of the clock.

Logic states are retained either High or Low according to the clock level.

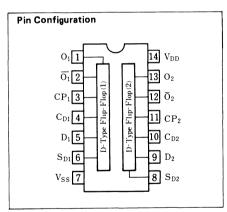
The MN4013B/S are equivalent to MOTOROLA MC14013B and RCA CD4013B.

## Truth Table

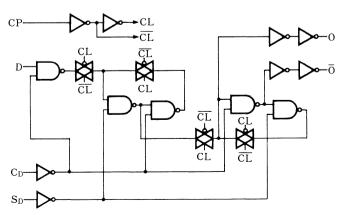
	Inp	out		Output			
Sp	Съ	CP	D	$O_{n+1}$	$\overline{O}_{n+1}$		
Н	L	×	×	Н	L		
L	Н	×	×	L	Н		
Н	Н	×	×	Н	Н		
L	L	~	×	On	$\overline{O}_n$		
L	L		L	L	Н		
L	L		Н	Н	L		

Note) X: don't care

# P- 1 14-Pin • Plastic DIL Package P- 2 14-Pin • Panaflat Package (SO-14D)



## Logic Diagram (1/2)



## Pin Explanation

S<sub>D</sub>: Data-set inputC<sub>D</sub>: Data-clear inputD: Data input

CP: Clock input

O,  $\overline{O}$ : Output (complementary)



## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperatur	re	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

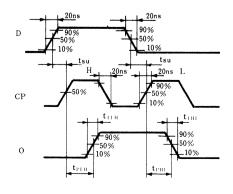
Y.	$V_{\mathrm{DD}}$	Sym-		2 114	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	
Item	(V)	bol	(	Conditions	min.	max.	min.	max.	min.	max.	Unit
Quiescent Power	5	_				4		4		30	
Supply Current	10	$I_{DD}$	$V_l = V_{SS}$ or	$V_{DD}$	-	8		8		60	μA
***************************************	15					16		16		120	
Output Voltage	5		$V_I = V_{SS}$ or	V <sub>DD</sub>		0.05		0.05		0.05	
Low Level	10	$V_{OI}$	$ I_0  < 1\mu A$			0.05		0.05		0.05	V
	15		1201 (27.11			0.05	-	0.05	*****	0.05	
Output Voltage	5		$V_{l} = V_{ssor}$	Vm	4.95		4.95	_	4.95		
High Level	10	$V_{OH}$	$ I_0  < 1\mu A$	עם י	9.95		9.95		9.95		V
15			10  < 1 mA	$ 1_0  < 1\mu$ A			14.95	********	14.95		
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =1V or 9V		3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4	_	4		4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4 \text{ V}$	V <sub>I</sub> =0 V or 5V	0.52		0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$	$V_1 = 0 \text{ V or } 10 \text{ V}$	1.3		1.1		0.9	-	mA
LOW LEVEL	15		$V_0 = 1.5 V_1$	$V_I = 0 \text{ V or } 15 \text{ V}$	3.6		3	*****	2.4		
	5		$V_0 = 4.6 V$	$V_1 = 0 \text{ V or } 5 \text{ V}$	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$	$V_1 = 0 \text{ V or } 10 \text{ V}$	1.3		1.1		0.9		mA
Iligii Level	15			$V_1 = 0 V \text{ or } 15 V$	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	V <sub>1</sub> =0V or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0V or	15 V		0.3	_	0.3		1	μA

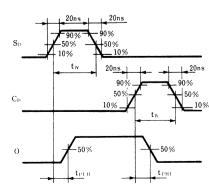
## ■ Switching Characteristics (Ta = 25°C, $V_{SS} = 0$ V, $C_L = 50$ pF)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time (Fig. 1)	10	t <sub>TIH</sub>	-	30	90	ns
_	15			20	60	
	5			60	180	
Output Fall Time (Fig. 2)	10	t <sub>THL</sub>	-	30	90	ns
	15			20	60	
	5		vanores	30	90	
Minimum Date Set-up Time	10	tsu		10	30	ns
	15			10	30	
	5		20		_	
Maximum Clock Rise Time Maximum Clock Fall Time	10	trø, tfø	2.5	_		μs
	15		1			
	5		6	12	_	
Maximum Clock Frequency	10	fmax	12	25		MHz
	15		18	36		
Propagation Delay Time (Fig. 1)	5			100	300	
(CP-O, $\bar{O}$ )	10	tplH		40	120	ns
(61 – 6, 6)	15			30	90	
Propagation Delay Time (Fig. 2)	5			110	330	
$(CP-O, \overline{O})$	10	t <sub>PHL</sub>	_	45	135	ns
(61 – 6, 6)	15		_	30	90	
Propagation Delay Time <sup>(Fig. 1)</sup>	5			135	405	
$(C_D, S_D-O, \overline{O})$	10	t <sub>PLH</sub>		50	150	ns
$(C_0, S_0-0, O)$	15		-	35	105	
Propagation Delay Time <sup>(Fig. 2)</sup>	5			100	300	
	10	t <sub>PHL</sub>		40	120	ns
$(C_D, S_D-O, \overline{O})$	15			30	90	
(Fig. 2)	5	4	_	45	135	
Minimum Clear Pulse Width (Fig. 2)	10	twcD	_	20	60	ns
Minimum Preset Pulse Width	15	twsn	_	20	60	
Input Capacitance		Ci	_		7.5	pF

## • Dynamic Signal Waveforms

 $(\text{Fig. 1}) \quad t_{\text{TLH}}, \, t_{\text{PLH}}(\text{CP-O}, \, \overline{O}) \,, \, t_{\text{PHL}}(\text{CP-O}, \, \overline{O}) \\ \quad \text{(Fig. 2)} \, t_{\text{PLH}}(S_{\text{D}}\text{-O} \,, \, C_{\text{D}}\text{-}\overline{O}) \,, \, t_{\text{PHL}}(S_{\text{D}}\text{-O} \,, \, C_{\text{D}}\text{-}\overline{O}) \,, \, t_{\text{WCD}}, \, t_{\text{WSD}} \\ \quad \text{(Fig. 2)} \, t_{\text{PLH}}(S_{\text{D}}\text{-O} \,, \, C_{\text{D}}\text{-}\overline{O}) \,, \, t_{\text{PHL}}(S_{\text{D}}\text{-O} \,, \, C_{\text{D}}\text{-}\overline{O}) \,, \, t_{\text{WCD}}, \, t_{\text{WSD}} \,, \, t_{\text$ 





# MN4015B/MN4015BS

## Dual 4-Stage Static Shift Registers

## Description

The MN4015B/S are dual 4-bit static shift registers.

Each register of D type flip-flop has a common reset input and can be cleared asynchronously, and triggered on the positive going edge of the clock.

A High on the reset input clears all registers and forces the outputs  $(O_0 \sim O_3)$  Low, independent of the clock and data inputs.

The MN4015B/S are equivalent to MOTOROLA MC14015B and RCA CD4015B.

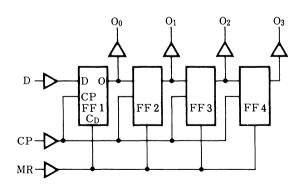
## Truth Table

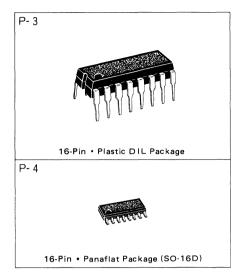
	Inp	ut		Output					
n	CP	D	MR	O <sub>0</sub>	O <sub>1</sub>	O2	O <sub>3</sub>		
1		$D_1$	L	$D_1$	×	×	×		
2	5	$D_2$	L	$D_2$	$D_1$	×	×		
3		$D_3$	L	$D_3$	$D_2$	$D_1$	×		
4		$D_4$	L	$D_4$	$D_3$	$D_2$	$D_1$		
	~	×	L	no change					
	×	×	Н	L	L	L	L		

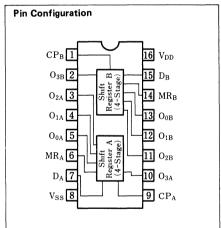
Note) X : don't care $D_n : High or Low$ 

n : Clock pulse count

## ■ Logic Diagram (1/2)







## Pin Explanation

D : Data input

 $\operatorname{CP}$  : Clock input (  $\mathcal{J}$  )

MR: Reset input

 $O_0 \sim O_3$ : Output (4 Bits)

## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	$^{\circ}$
Storage Temperatur	e	Tstg	$-65\sim+150$	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

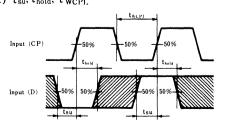
•	$V_{\mathrm{DD}}$	Svm-		1	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	T T ! 4
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
	5				_	20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40	_	300	μA
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	<b>V</b> DD		0.05	_	0.05	_	0.05	V
Eow Eover	15		$ 10  < 1\mu A$	<1μA		0.05		0.05		0.05	
	5		$V_I = V_{SS}$ or	V	4.95	_	4.95	_	4.95	-	
Output Voltage High Level	10	$V_{OH}$	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	$\mathbf{v}_{\mathrm{DD}}$	9.95	_	9.95		9.95	-	V
	15		1 <sub>0</sub>   < 1μΛ		14.95	_	14.95		14.95		
	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V		3	_	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
I	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7	_	7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4 V$	$V_I = 0 V \text{ or } 5V$	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_l = 0 V \text{ or } 10V$	1.3		1.1		0.9	-	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 V \text{ or } 15V$	3.6		3	_	2.4		
	5		$V_0 = 4.6 V$	$V_I = 0 V \text{ or } 5 V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_l = 0 V \text{ or } 10 V$	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 13.5 V$	, $V_1 = 0 V$ or $15 V$	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I = 0 V \text{ or } 5 V$	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_l = 0V$ or	15 V	_	0.3		0.3		1	μA



Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time	10	tTHL	_	30	90	ns
	15			20	60	
	5		_	145	435	
Propagation Delay Time	10	t <sub>PHL</sub>		60	180	ns
CP—On(H→L)	15			40	120	
Description Delay Time	5			120	360	
Propagation Delay Time	10	tplH	_	55	165	ns
$CP-On(L\rightarrow H)$	15		_	40	120	
	5			185	555	
Propagation Delay Time	10	tphL	_	70	210	ns
MR→On(H→L)	15	1	_	40	120	
(Fig. 1)	5	<del> </del>		55	166	
Set-up Time (Fig. 1)	10	tsu		15	45	ns
D→CP	15			10	30	
(Ft. 4)	5	<u> </u>		20	60	
Hold Time (Fig. 1)	10	thold	_	10	30	ns
D→CP	15	Chota	_	8	24	
	5			50	150	
(Fig. 1) Minimum Clock Pulse Width	10	t WCPL		20	60	ns
	15	ewer.	_	15	45	
(FI. 2)	5			55	165	-
(Fig. 2) Minimum Reset Pulse Width	10	twmrh	_	20	60	ns
	15	WMKH		15	45	
	5	<del> </del>		65	195	
Reset Recovery Time (Fig. 2)	10	t <sub>RMR</sub>	_	20	60	ns
Reset Recovery Time (Fig. 2)	15	CKMK	_	15	45	5
	5		4	9		
Maximum Clock Frequency	10	fmax	12	23		MHz
aximum Clock Frequency	15	Illiax	17	34	_	141112
Input Capacitance	10	Cı	11		7.5	pF

## • Dynamic Signal Waveforms

(Fig. 1) t<sub>su</sub>, t<sub>hold</sub>, t<sub>WCPL</sub>



Waveforms showing set-up times, hold times and minimum clock pulse width

(Fig. 2) t<sub>WMRH</sub>, t<sub>RMR</sub>

Input (MR)

Input (CP)

Output

Waveforms showing recovery time for MR and minimum MR pulse width

# MN4016B/MN4016BS

## Quad Analog Switches

## Description

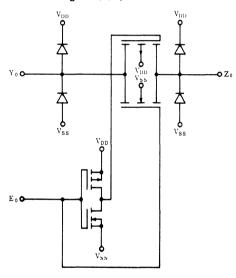
The MN4016B/S have 4 independent analog switches. A High on the enable input establishes a low impedance state (ON stage) between input and output of the switch.

A Low produces a high impedance (OFF state).

This can be utilized for analog or digital signal switching and for choppers, modulators and demodulators.

The MN4016B/S are equivalent to MOTOROLA MC14016B and RCA CD4016B.

## Schematic Diagram (1/4)



## Pin Explanation

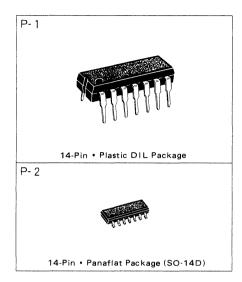
 $E_0{\sim}E_3$ : Enable input  $Z_0{\sim}Z_3$ : Analog input/output

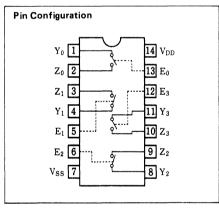
 $Y_0\!\sim\!Y_3$  : Analog input/output

## $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	-0.5~V <sub>DD</sub> +0.5*	V
Output Voltage		$V_{0}$	-0.5~V <sub>DD</sub> +0.5*	V
Peak Input · Output Current		$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperatur	re	Tstg	-65~+150	°C

 $<sup>*</sup>V_{DD} + 0.5V$  should be under 18V







## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Ta=	<b>25</b> ℃	Ta=	85℃	Unit
	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Ont
Oning and Barrer	5				_	1		1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		2		2 ,		15	μA
	15				-	4	_	4		30	
	5			$V_0 = 0.5 V \text{ or } 4.5 V$	-	1.5	********	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3		3	v
Dow Bever	15			$V_0 = 1.5 V \text{ or } 13.5 V$		4		4		4	
	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5	_	3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$	7	_	7		7		V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$	11		11		11	_	
Input Leakage Current	15	$\pm I_{I}$	V <sub>i</sub> =0 or 15	V	_	0.3		0.3		1	μA

## 

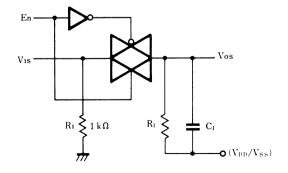
Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit	
			$V_{SS}=0V$ , $V_{I}=5V$	_	200			
	5	R <sub>on</sub>	$V_{SS}=0V$ , $V_{I}=2.5V$	_	8000		Ω	
			$V_{SS} = 0V, V_{I} = 0.25V$		200			
		Ron	$V_{SS}=0V$ , $V_{I}=10V$		150	700		
	10		$V_{SS}=0V$ , $V_{I}=5V$		250	1500	Ω	
			$V_{SS} = 0V, V_I = 0.25V$		150	700		
On Resistance	15		$V_{SS}=0V$ , $V_I=15V$		100	500		
		R <sub>ON</sub>	$V_{SS} = 0V, V_{I} = 7.5V$		200	950	Ω	
			$V_{SS} = 0V, V_{I} = 0.25V$	_	100	500		
		Ron	$V_{SS} = -5V$ , $V_I = 5V$	-	150	700		
	5		$V_{SS} = -5V, V_I = \pm 0.25V$	-	250	1500	Ω	
			$V_{SS} = -5V$ , $V_I = -5V$	_	150	700		
			$V_{SS} = -7.5V, V_{I} = 7.5V$		100	500		
	7.5	Ron	$V_{SS} = -7.5V, V_I = \pm 0.25V$		200	950	Ω	
			$V_{SS} = -7.5V, V_{I} = -7.5V$		100	500		
	10		$V_{I}=10V, V_{O}=0V$	_	30	125	nA	
Input/Output of leakage current	10	_	$V_{I}$ =0V, $V_{O}$ =10V		30	125	nA	
	15	I <sub>OFF</sub>	$V_I=15V, V_O=0V$		60	250	- 1	
	15		$V_I$ =0V, $V_O$ =15V		60	250	nA	

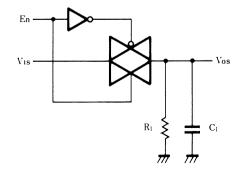
## 

Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1)	5			_	25	75	
(Vis→V <sub>OS</sub> )	10	t <sub>PHL</sub>	$R_L = 10 k\Omega$	_	10	30	ns
	15		$C_L = 50 \text{pF}$	_	5	15	
Propagation Delay Time (Fig. 1)	5		$E_D = V_{DD}$	_	20	60	
(V <sub>1s</sub> →V <sub>OS</sub> )	10	tPLH	Eu - App	_	10	30	ns
(VIS VOS)	15			_	5	15	
Propagation Delay Time (Fig. 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	95	285	
	10	tPHZ			85	255	ns
$(En \rightarrow V_{OS})$ (H)	15		$Vis = V_{DD}, R_L \rightarrow V_{SS}$	_	85	255	
(Fig. 1)	5		D 1010 C 50 E	_	50	150	
Propagation Delay Time (Fig. 1)	10	tPLZ	$R_L = 10k\Omega$ , $C_L = 50pF$	_	55	165	ns
$(En \rightarrow V_{OS})$ (L)	15		$Vis = V_{SS}, R_L \rightarrow V_{DD}$	_	60	180	
(Fig. 1)	5		$\begin{aligned} R_L = & 10k\Omega, & C_L = & 50pF \\ V_{1S} = & V_{DD}, & R_L \rightarrow & V_{SS} \end{aligned}$	_	35	105	
Propagation Delay Time (Fig. 1)	10	t <sub>PZH</sub>		_	20	60	ns
$(En \rightarrow V_{OS})$ (H)	15			_	15	45	
Fig 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	35	105	
Propagation Delay Time (Fig. 1)	10	tPZL		_	15	45	ns
$(En \rightarrow V_{OS})$ (L)	15		$Vis = V_{SS}, R_L \rightarrow V_{DD}$	_	10	30	
	5		$R_L = 10k\Omega$ , $C_L = 15pF$		_		
Sine Wave Distortion (Fig. 2)	10		$En = V_{DD}, f = 1 \text{ kHz}$	_	0.1	-	%
	15		$Vis = \frac{1}{2} V_{DD} (P-P)$	_	0.1	_	
	5		B 110	_		_	
Crosstalk (Fig. 3)	10		$R_L = 1 k\Omega$	_	1	_	MHz
(Between 2 Channels)	15		$Vis = \frac{1}{2} V_{DD} P_{PP}$			_	
(Fig. 1)	5		$R_L = 10k\Omega$	_		- Managara	
Crosstalk (Fig. 1) (En→V <sub>OS</sub> )	10		$C_1 = 15pF$	_	80	_	mV
	15		$En = V_{DD}$		_	_	
	5		$R_L = 1 k\Omega$ , $C_1 = 5 pF$	_		_	
Feedthrough (Fig. 2)	10		$En = V_{SS}$	_	700	_	kHz
(OFF)	15		$Vis = \frac{1}{2}V_{DD}, P_{-P}$	-	_	_	
Input Capacitance		Cı		_	_	7.5	pF

Fig. 1 Propagation Crosstalk Test Circuit

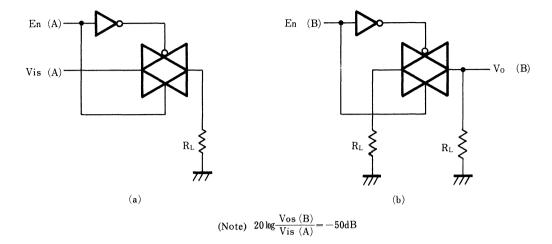
Fig. 2 Sine Wave Distortion, Feedthrough Test Circuit



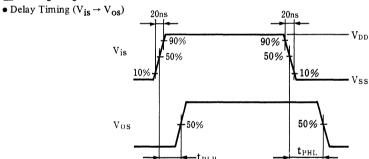


$$(Note) \qquad 20 \, \log \frac{\mathrm{Vos}}{\mathrm{V1s}} = -50 \mathrm{dB}$$

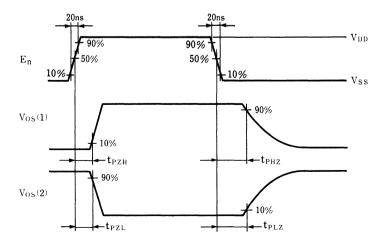
Fig. 3 Crosstalk Test Circuit



## Timing Diagram



## • Chip Enable Timing Diagram



# MN4017B/MN4017BS

## 5-Stage Johnson Counters

## Description

The MN4017B/S are 5-stage Johnson decade counters constructed with five D-type flip-flops. One of the outputs ( $O_0 \sim O_9$ ) becomes High level according to the number of counter pulses applied to  $CP_0$  or  $\overline{CP}_1$ . The counter is advanced by either a positive going edge of  $CP_0$  while  $\overline{CP}_1$  is Low or a negative going edge of  $\overline{CP}_1$  while  $CP_0$  is High. A High on the reset input (MR) resets the counter to zero ( $O_0 = \overline{O}_{5-9} = \text{High}$ ,  $O_1 \sim O_9 = \text{Low}$ ) independent of the clock inputs ( $CP_0$ ,  $\overline{CP}_1$ ).

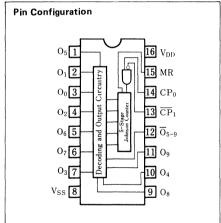
These are equivalent to MOTOROLA MC14017B and RCA CD4017B.

## ■ Truth Table

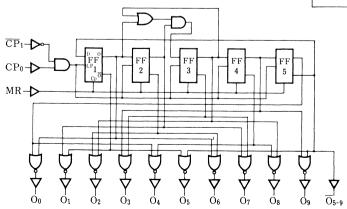
MR	CP <sub>0</sub>	$\overline{CP}_1$	Mode
Н	×	×	$O_0 = \overline{O}_5 = H$ , $O_1 \sim O_9 = L$
L	Н	_	Counter Advances
L		L	Counter Advances
L	L	×	
L	×	Н	No Change
L	Н		No Change
L	_	L	

Note) X: don't care

# P- 3 16-Pin • Plastic DIL Package P- 4 16-Pin • Panaflat Package (SO-16D)



## Logic Diagram



## Pin Explanation

 $CP_0$ : Positive clock input ( $\mathcal{L}$ )  $\overline{CP}_1$ : Negative clock input ( $\mathcal{L}$ )

MR : Reset input  $O_0 \sim O_9$  : Output (10 Bits)

## ■ Maximum Ratings (Ta=25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	$-0.5\sim +18$	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	337
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	−65~+150	C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

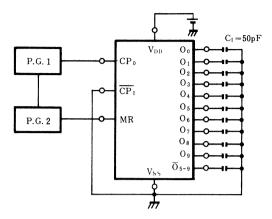
Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	Ta=-40℃		25℃	Ta=85℃		Unit
item (		bol		Conditions		max.	min.	max.	min.	max.	Unit
O. i	5					20		20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{\mathrm{DD}}$		40		40		300	$\mu$ A
	15					80		80		600	
	5		V - V	17		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	V <sub>DD</sub>	_	0.05		0.05		0.05	V
Low Level	15		$ I_{\rm O}  < 1\mu A$		_	0.05		0.05		0.05	
	5		17 - 17	17	4.95		4.95		4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or	$V_{ m DD}$	9.95		9.95		9.95		V
	15		$ I_0  < 1\mu A$	uA		_	14.95	_	14.95	-	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
	5		$ I_0  < 1\mu A$	Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5		
Input Voltage High Level	10	$V_{IH}$		Vo=1V or 9V	7	_	7	_	7		V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$	11		11		11		
	5		$V_0 = 0.4 V$	$V_l = 0 \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9		mA
Low Lover	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6	_	3	_	2.4		
_	5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5 $V$	0.52	_	0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I {=} 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9	_	mA
High Level	15		$V_0 = 13.5 \text{ V}$	, $V_I$ =0 or 15 $V$	3.6		3	_	2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>i</sub> =0 or 15	5V		0.3	_	0.3	_	1	μA

## 

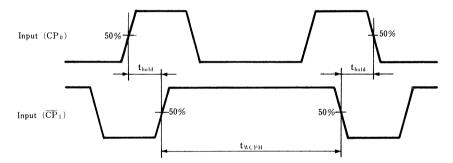
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>TH1</sub>	_	30	90	ns
	15		_	20	60	
D D 1	5		_	195	585	
Propagation Delay Time	10	t <sub>PHI</sub>		75	225	ns
$CP_0, \overline{CP}_1 \rightarrow O_0 \text{ to } O_9 \text{ (H}\rightarrow L)$	15			50	150	
D D MI	5		_	245	735	,
Propagation Delay Time	10	t <sub>PLH</sub>		95	285	ns
$CP_0, \overline{CP}_1 \rightarrow O_0 \text{ to } O_9 \text{ (L} \rightarrow H)$	15	T E II	_	60	180	
	5		_	245	735	
Propagation Delay Time	10	t <sub>PHL</sub>	-	90	270	ns
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5-9} (H \rightarrow L)$	15	FAL		60	180	
	5		_	190	570	
Propagation Delay Time	10	t <sub>PLH</sub>		75	225	ns
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5-9} (L \rightarrow H)$	15	• РЕН		50	150	115
	5		_	130	390	
Propagation Delay Time	10			55		
$MR \rightarrow O_1$ to $O_9$ $(H \rightarrow L)$		t <sub>PHL</sub>			165	ns
	15			40	120	
Propagation Delay Time	5	,		110	330	
$MR \rightarrow \overline{O}_{5-9} (L \rightarrow H)$	10	$t_{ ext{PLH}}$	_	45	135	ns
	15		_	35	105	
Propagation Delay Time	5		_	130	390	
$MR \rightarrow O_0 \ (L \rightarrow H)$	10	t <sub>PLH</sub>		55	165	ns
	15			40	120	
Hold Time	5		_	70	210	
$CP_0 \rightarrow \overline{CP}_1$	10	thold	_	25	75	ns
	15			15	45	
Hold Time	5		_	85	255	
$\overline{CP}_1 \rightarrow CP_0$	10	thold	_	30	90	ns
	15			20	60	
	5		_	35	105	
Minimum Clock Pulse Width	10	$t_{\mathrm{WCP}}$	_	15	45	ns
	15		-	10	30	
	5		_	35	105	
Minimum Reset Pulse Width	10	twmrh		15	45	ns
	15		_	10	30	
	5			25	75	
Reset Recovery Time	10	$t_{RMR}$		10	40	ns
	15		_	10	30	
	5		3	6		
Maximum Clock Frequency	10	fmax	8	16	_	ns
· · · · · · · · · · · · · · · · ·	15		12	24	_	
Input Capacitance		C <sub>I</sub>	_		7.5	pF



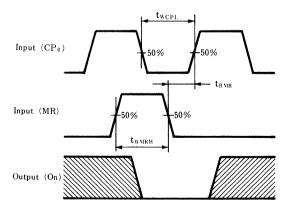
## 1. Switching Time Test Circuit



## 2. Waveforms



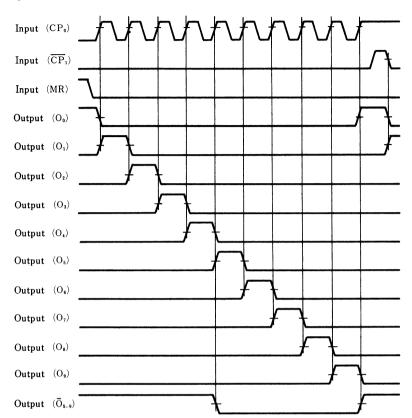
Waveforms showing hold times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to  $CP_0$ Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum  $CP_0$  and MR pulse widths Conditions:  $\overline{CP}_1 = LOW$  while  $CP_0$  is triggered on a LOW to HIGH transition;  $t_{WCP}$  and  $t_{RMR}$  also apply when  $CP_0 = HIGH$  and  $\overline{CP}_1$  is triggered on a HIGH to LOW transition.

CAMACANIA . A A

## ■ Timing Diagram





# MN4018B/MN4018BS

Presettable Divide-by-N Counters

## Description

The MN4018B/S are presettable divide-by-N counters composed of a 5-bit Johnson counter.

Frequency is divided into 1/2, 1/4, 1/6, 1/8 and 1/10 by connecting the output of  $\overline{O_0} \sim \overline{O_4}$  to D input, and frequency is also divided into 1/3, 1/5, 1/7 and 1/9 by connecting the output of  $\overline{O_0} \sim \overline{O_4}$  to the D input through gate.

MR and PL are asynchronous. When MR = "H",  $\overline{O}_0 \sim \overline{O}_4$  are all "H"; when PL = "H", On is contradiction of Pn.

Counter advances by one on the going edge of CP input. Proper counter sequence is given since the lock protection gate is available.

The MN4018B/S are equivalent to MOTOROLA MC14018B and RCA CD4018B.

## Truth Table

CP	MR	PL	P <sub>0</sub> ~P <sub>4</sub>	$\overline{O}_n$
	L	L	×	$\overline{O}_n$
	L	L	×	$\overline{\mathrm{D}}_{\mathrm{n}}$
×	L	Н	L	Н
×	L	Н	Н	L
×	Н	×	×	Н

Note) X: don't care

## Functional Selection Table

Dividing number	Output to D	Remarks
10 8 6 4 2	$\begin{array}{c} \overline{O}_4 \\ \overline{O}_3 \\ \overline{O}_2 \\ \overline{O}_1 \\ \overline{O}_0 \end{array}$	External connection is not necessary
9 7 5 3	$\begin{array}{c} \overline{\mathrm{O}}_3 \cdot \overline{\mathrm{O}}_4 \\ \overline{\mathrm{O}}_2 \cdot \overline{\mathrm{O}}_3 \\ \overline{\mathrm{O}}_1 \cdot \overline{\mathrm{O}}_2 \\ \overline{\mathrm{O}}_0 \cdot \overline{\mathrm{O}}_1 \end{array}$	External AND gate is necessary

## Pin Explanation

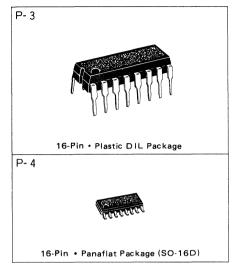
PL: Load input  $P_0 \sim P_4$ : 4-bit input

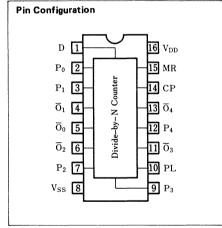
D : Data input

CP: Clock input (\_/\_)

MR: Reset input

 $\overline{\mathrm{O}}_0{\sim}\overline{\mathrm{O}}_4$ : Output (4 bit)





## ■ Maximum Ratings (Ta=25°C)

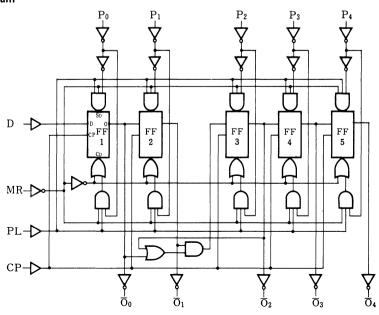
Item		Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		Vi	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{\rm I}$	max. 10	mA
Power Dissipation Ta=-40~+60°C		D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

T+	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=25℃		Ta=85℃		Unit
Item	(V)	bol		conditions	min.	max.	min.	max.	min.	max.	Unit
O : + P	5				_	20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40	_	40	_	300	μA
Supply Culture	15				_	80	_	80	_	600	
	5		V — V	17		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	V <sub>DD</sub>	_	0.05	l — i	0.05		0.05	v
Low Level	15		$ I_0  < 1\mu A$	:	_	0.05	_	0.05	_	0.05	
	5			17	4.95	_	4.95		4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	$V_{ m DD}$	9.95	_	9.95	_	9.95	_	V
Then bever	15		$ 1_0  < 1 \mu A$	$ I_0  < 1 \mu A$			14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V		3		3		3	v
Low Level	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4	_	4	_	4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5	_	3.5	_	
Input Voltage High Level	10	VIH	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	v
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11	_	11	_	
	5		$V_0 = 0.4 V$	V <sub>I</sub> =0 or 5V	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I{=}0\ or\ 10\text{V}$	1.3	_	1.1	_	0.9	_	mA
Low Level	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6	_	3	_	2.4		
	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44	_	0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3	_	1.1	_	0.9		mA
II.g.i Dovoi	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6		3		2.4	_	
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	$V_{\rm i} = 0 \text{ or } 15$	iV	_	0.3	_	0.3	_	1	μA

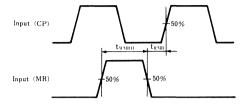
## Logic Diagram



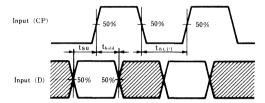
■ Switching Characteristics  $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$ 

Switching Characteristics	(1a=25C,	vss=uv, c	L=50pF			
Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
***************************************	5			60	180	
Output Rise Time	10	$t_{TLH}$	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Propagation Delay Time	5		_	185	555	
CP→Ō (H→L)	10	$t_{ ext{PHL}}$	_	65	195	ns
	15			50	150	
Propagation Delay Time	5		_	145	435	
CP→Ō (L→H)	10	$t_{\mathtt{PLH}}$	_	55	165	ns
Cr → O (L → n)	15			40	120	
Propagation Delay Time	5			205	615	
PL→ <del>O</del> (H→L)	10	$\mathbf{t}_{\mathtt{PHL}}$	_	70	210	ns
FL→O (n→L)	15			50	150	
Propagation Delay Time	5			175	525	
PL→Ō (L→H)	10	$t_{ m PLH}$		65	195	ns
PL→O (L→H)	15		_	50	150	
Propagation Delay Time	5			140	420	
	10	$t_{\rm PLH}$	-	55	165	ns
$MR \rightarrow \overline{O} (L \rightarrow H)$	15			40	120	
Sat un Tima	5			65	195	
Set-up Time	10	tsu	_	20	60	ns
D→CP	15			15	45	
xr 11 m'	5			<b>-45</b>	30	
Hold Time	10	thold	_	-15	10	ns
D→CP	15		Magnitudes	-10	10	
	5		-	70	210	
Minimum Clock Pulse Width	10	twcpl		25	75	ns
	15		_	20	60	
	5		_	50	150	
Minimum MR Pulse Width	10	twmrh	_	20	60	ns
	15			15	45	
	5			75	225	
Minimum PL Pulse Width	10	twPLH		25	75	ns
	15		_	20	60	
	5		<del>-</del>	70	210	
MR Recovery Time	10	t <sub>RMR</sub>	_	20	60	ns
	15		_	15	45	
PL Recovery Time	5		_	85	255	
	10	t <sub>RPL</sub>	-	30	90	ns
	15		_	20	60	
	5		2	4	_	
Maximum Clock Frequency	10	fmax	6	11		MHz
	15		8	16		
Input Capacitance		Ci	_		7.5	pF

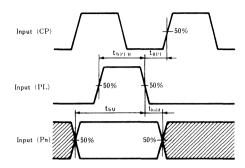
## • Dynamic Signal Waveforms



Waveforms showing minimum MR pulse width and MR recovery time

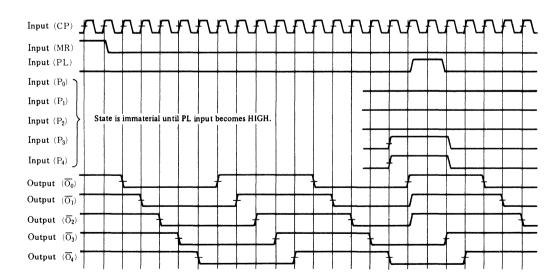


Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D  $\,$ 



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for Pn to PL; set-up and hold times are shown as positive values but may be specified as negative values.

## Timing Diagram



# MN4019B/MN4019BS

### Quad 2-Input Multiplexers

### Description

The MN4019B/S are quad 2-input multiplexers composed of two 2-input AND gates and 0R gate with its two outputs.

The inputs applied to A and B are output to X selected by select input  $(S_A, S_B)$  common to 4 circuits.

These are equivalent to RCA CD4019B.

### Truth Table

Select	Input	Inp	ut	Output
SA	SB	A	В	0
L	L	×	×	L
Н	L	L	×	L
Н	L	Н	×	Н
L	Н	×	L	L
L	Н	×	Н	Н
Н	Н	Н	×	Н
Н	Н	×	Н	Н
Н	Н	L	L	L

Note) X: don't care

### Pin Explanation

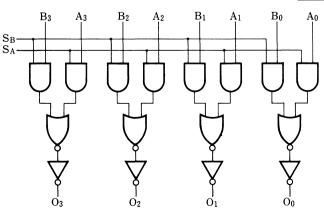
SA, SB: Select input

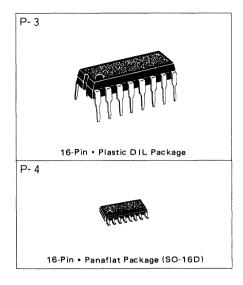
A<sub>0</sub>~A<sub>3</sub>: Input

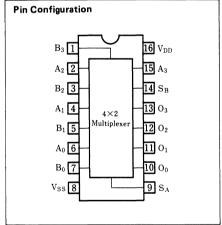
 $B_0 \sim B_3$ : Input

O<sub>0</sub>~O<sub>3</sub>: Output

### Logic Diagram







### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{ m DD}$	-0.5∼+18	V	
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output	Current	$\pm I_{I}$	max. 10	mA	
Power Dissipation	Ta=-40~+60°C	- D	max. 400	117	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (1	per output terminal)	$P_D$	max. 100	mW	
Operating Ambient	Temperature	Topr	-40~+85	$^{\circ}$	
Storage Temperatur	e	Tstg	<del>-65</del> ∼+150	°C	

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

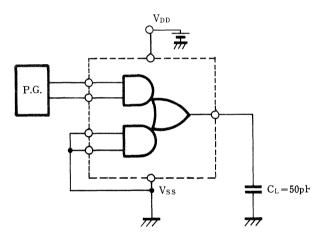
## $\blacksquare$ DC Characteristics $(V_{SS} \! = \! 0V)$

***	$V_{\mathrm{DD}}$	Sym-		1 - 4:4:	Ta=-	-40°C	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
O :	5					20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I}=V_{SS}$ or	$V_{DD}$	-	40		40	_	300	μA
	15				_	80		80	_	600	
_	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	$V_{OL}$	$ V_1 - V_{SS} $ or $ I_0  < 1\mu$ A	VDD	_	0.05		0.05		0.05	V
	15		10  \ 1 \mu A		_	0.05		0.05	_	0.05	
0-1-17	5		V – V	V	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	$V_{OH}$	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	V <sub>DD</sub>	9.95	_	9.95		9.95	_	v
	15		10  < 1 µ A		14.95		14.95	_	14.95	_	
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	-	1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	-	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4	_	4	
Input Voltage	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5		3.5		
High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7		v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
0 0	5		$V_0=0.4V$ ,	$V_I = 0$ or $5V$	0.52	_	0.44		0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	-	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4	_	
Outroot Comment	5		$V_0=4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9	_	mA
Iligii Level	15		$V_0 = 13.5 V$	, V₁=0 or 15V	3.6		3		2.4		
Output Current High Level	5	−I <sub>OH</sub>	$V_0=2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{t}$	$V_1 = 0 \text{ or } 15$	SV		0.3		0.3	_	1	μA

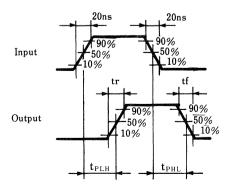
### Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		-	20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5			60	180	
Propagation Delay Time	10	t <sub>PLH</sub>		25	75	ns
$(An, Bn, S_A, S_B-On)$	15			15	45	
D D 1	5			70	210	
Propagation Delay Time	10	t <sub>PHL</sub>	_	30	90	ns
$(An, Bn, S_A, S_B-On)$	15			25	75	
Input Capacitance		Cı			7.5	pF

### 1. Switching Time Test Circuit



### 2. Waveforms



# MN4020B/MN4020BS

# 14-Stage Binary Counters

### Description

The MN4020B/S are binary counters in which an input-shaping circuit and 14-Stage flip-flops are built in.

Count is performed on the negative going edge of clock input. The MN4020B/S are equivalent to MOTOROLA MC14020B and RCA CD4020B.

### Truth Table

CP	MR	Mode
	L	No Change
	L	Counter Advance
×	Н	O <sub>0</sub> ~O <sub>13</sub> =All "L"

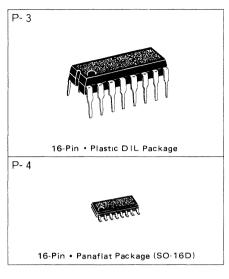
Note) X: don't care

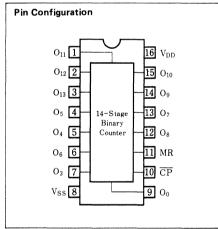
### Pin Explanation

 $\overline{\mbox{CP}}$  : Negative clock input

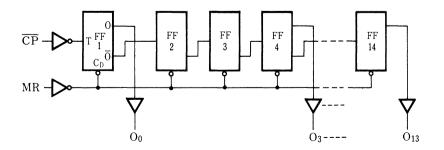
MR: Reset input

 $O_0, O_3{\sim}O_{13}$  : Parallel output





### Logic Diagram





### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit			
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V			
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V			
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V			
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA			
Power Dissipation	Ta=-40~+60℃	D.	max. 400				
(per package)	Ta=+60~+85℃	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW			
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW			
Operating Ambient	Temperature	Topr	-40~+85	°C			
Storage Temperatur	re	Tstg	-65~+150	°C			

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

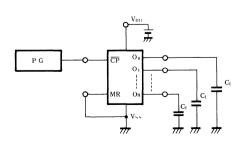
### $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	$V_{\mathrm{DD}}$	Sym-	(	Conditions	$T_a = -$	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
Ttem	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Ont
0 :	5				_	20		20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or $V_{DD}$			40	_	40		300	μA
Suff.y Switten	15					80		80	_	600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol		$ I_0  < 1 \mu A$		0.05		0.05		0.05	V
East East	15		101 ~ 1 MA		_	0.05	_	0.05		0.05	
	5		$V_1 = V_{SS}$ or	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	VoH	$V_1 = V_{SS}$ or $ I_0  < 1 \mu A$	VDD	9.95		9.95		9.95	_	V
	15		10  \ 1 \mu A		14.95		14.95	_	14.95		
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	-	3	-	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
Toward Wolfers	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5		3.5		3.5		
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11		
0 0	5		$V_0 = 0.4V$	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36	_	
Output Current Low Level	10	I <sub>oL</sub>	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1	_	0.9	_	mA
	15		$V_0 = 1.5V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
	5		$V_0=4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	−I <sub>OH</sub>	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9		mA
High Level	15		$V_0 = 13.5 V$	, V <sub>l</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_{i} = 0 \text{ or } 15$	SV		0.3		0.3	_	1	μA

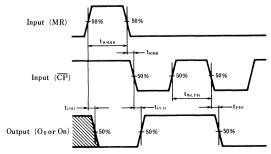
### ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF')$

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TIH</sub>		30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Dti D-1 Ti	5			105	315	
Propagation Delay Time $\overline{CP} \rightarrow O_0  (H \rightarrow L)$	10	t <sub>PHL</sub>		45	135	ns
$CP \rightarrow O_0  (H \rightarrow L)$	15		-	30	90	
Propagation Delay Time	5			105	315	
$\overline{CP} \rightarrow O_0  (L \rightarrow H)$	10	t <sub>Pl H</sub>		50	150	ns
$CP \rightarrow O_0  (L \rightarrow H)$	15			35	105	
Propagation Delay Time	5			80	270	
On→On +1 (H→L)	10	t <sub>PHI</sub>	-	30	90	ns
$On \rightarrow On + 1  (H \rightarrow L)$	15		-	20	60	
Propagation Delay Time On→On - 1 (L→H)	5		_	70	210	
	10	t <sub>PLH</sub>	-	25	75	ns
	15			20	60	
Propagation Delay Time	5			180	540	
	10	t <sub>PHL</sub>		90	270	ns
$MR \rightarrow On (H \rightarrow L)$	15			70	210	
	5			25	75	
Minimum Clock Pulse Width	10	twcph		15	45	ns
	15		_	10	30	
	5		_	65	195	
Minimum MR Pulse Width	10	twmRH		50	150	ns
	15		_	45	135	
	5		-	60	180	
Reset Recovery Time	10	t <sub>RMR</sub>	_	35	105	ns
	15			25	75	
	5		5	10	_	
Maximum Clock Frequency	10	fmax	13	25	_	MHz
	15		18	35		
Input Capacitance		Cı	-		7.5	pF

### 1. Switching Time Test Circuit

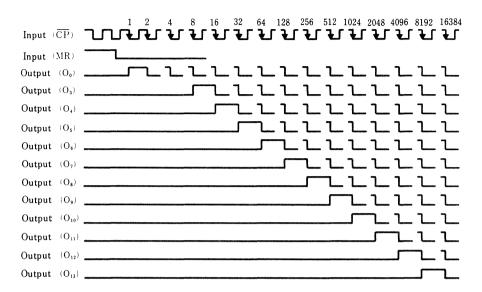


### 2. Waveforms



Waveforms showing propagation delays for MR to  $O_n$  and  $\overline{CP}$  to  $O_0$  , minimum MR and  $\overline{CP}$  pulse widths

### Timing Diagram



# MN4021B/MN4021BS

### 8-Bit Static Shift Registers

### Description

The MN4021B/S are 8-bit static shift registers composed of 8 register cells with its own parallel input.

Parallel input/series output and parallel input-series output conversion are enabled on the clock synchronization by controlling parallel/series control input (PL).

### Truth Table

### Serial Action

		Input		Output				
n	CP	Ds	PL	O <sub>5</sub>	$O_6$	O,		
1		$D_1$	L	×	×	×		
2		$D_2$	L	×	×	×		
3		$D_3$	L	×	×	×		
6		×	L	D <sub>1</sub> ×		×		
7		×	L	$D_2$	$D_1$	×		
8		×	L	$D_3$	$D_2$	$\mathbf{D}_1$		
	~	×	L	no change				

### Parallel Action

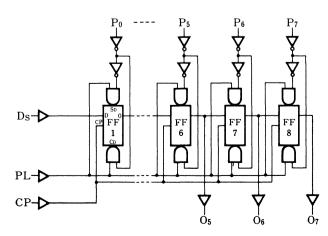
		Input		Output				
n	CP	Ds	PL	Os	O <sub>5</sub> O <sub>6</sub>			
	×	×	Н	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>		

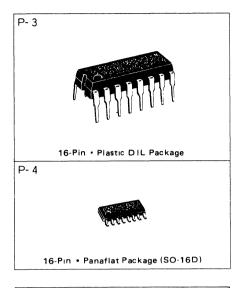
Note) X: don't care

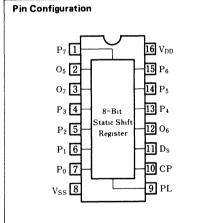
 $D_n$ : H or L

n": Clock pulse number

### Logic Diagram









### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{\rm o}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	137
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (1	per output terminal)	$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	re e	Tstg	<del>-65~+150</del>	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

	$V_{\mathrm{DD}}$	Sym-			Ta=-	-40°C	Ta=	25℃	Ta=	85℃	
Item	(X)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0	5					20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or V <sub>DD</sub>		_	40	_	40		300	$\mu$ A
Supply Culture	15					80	_	80	_	600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	$V_{OL}$	$ V_1 - V_{SS} $ or $ I_0  < 1\mu A$	VDD	_	0.05	_	0.05		0.05	V
25 25	15		10  \ 1 \mu A		_	0.05		0.05		0.05	
O	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95	_	4.95		4.95	_	
Output Voltage High Level	10	VoH	$v_I = v_{SS}$ or $ I_O  < 1 \mu A$	VDD	9.95	_	9.95	_	9.95	_	V
	15		10  < 1μΛ		14.95		14.95		14.95		
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	_	1.5		1.5		1.5	
Input Voltage Low Level	10	V <sub>II</sub> .	$ I_0  < 1\mu A$	V <sub>O</sub> =1V or 9V		3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4	_	4		4	
Imput Valtage	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	V <sub>O</sub> =1V or 9V	7	_	7	_	7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11	_	
	5		$V_0=0.4V$	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Outroot Command	5		$V_0 = 4.6 V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>		$V_I = 0 \text{ or } 10 \text{V}$	1.3	<u> </u>	1.1	_	0.9	_	mA
Ilikii Feaci	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	—I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>1</sub> =0 or 15	SV	-	0.3	_	0.3		1	μA

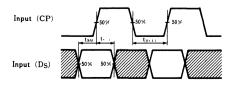
### 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit	
Output Rise Time	5			60	180		
	10	t <sub>TLH</sub>		30	90	ns	
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>		30	90	ns	
	15		_	20	60		

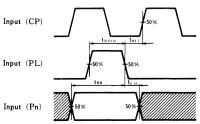
### ■ Switching Characteristics $(T_a = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$ (Continued)

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	170	510	
CP→On (H→L)	10	t <sub>PHL</sub>	_	65	195	ns
CP→On (H→L)	15		_	45	135	
Propagation Delay Time	5		_	130	390	
	10	t <sub>PLH</sub>		55	165	ns
$CP \rightarrow On (L \rightarrow H)$	15		_	40	120	
Propagation Delay Time	5		_	240	720	
	10	t <sub>PHL</sub>	_	90	270	ns
$PL \rightarrow On (H \rightarrow L)$	15		_	60	180	
Propagation Delay Time	5		_	175	525	
	10	t <sub>PLH</sub>	_	70	210	ns
$PL \rightarrow On (L \rightarrow H)$	15		_	50	150	
C-4 T:	5		_	45	135	
Set-up Time	10	tsu		15	45	ns
Ds→CP	15		_	10	30	
Sat-un Tima	5		_	70	210	
Set-up Time Pn→PL	10	tsu	_	25	75	ns
	15		_	20	60	
Hold Time	5			20	60	
	10	thold	_	10	30	ns
Ds→CP	15		_	8	24	
Hald Time	5		_	-10	24	
Hold Time	10	thold	_	0	24	ns
Pn→PL	15		_	0	24	
	5			55	165	
Minimum Clock Pulse Width	10	t <sub>WCPL</sub>	_	20	60	ns
	15		_	15	45	
	5		_	75	225	
Minimum PL Pulse Width	10	t <sub>WPIH</sub>	_	25	75	ns
	15			20	60	
	5		_	65	195	
PL Recovery Time	10	t <sub>RPL</sub>	_	20	60	ns
	15		_	15	45	
	5		4	9	_	
Maximum Clock Frequency	10	fmax	12	25	_	MHz
	15		18	37	_	,
Input Capacitance		Cı		_	7.5	pF

### • Dynamic Signal Waveforms



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and  $\mathsf{D}_{\mathsf{S}}$ 



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for  $P_n$  to PL; set-up and hold times are shown as positive values but may be specified as negative values.

# MN4022B/MN4022BS

# 4-Stage Divide-by-8 Johnson Counters

### Description

The MN4022B/S are octal Johnson counters constructed with 4-stage D-type flip-flops.

The built-in decoder converts output to the coal number.

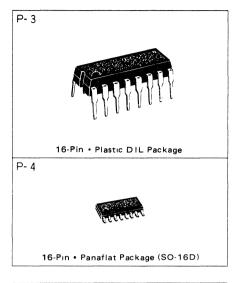
One output of 8 outputs  $(O_0 \sim O_7)$  becomes "H" by the count pulse added to  $CP_0$  and  $\overline{CP}_1$ .

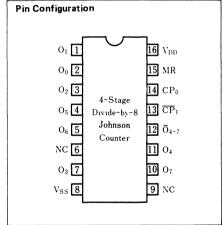
Count advances the count on the positive going edge of  $\overline{CP}_0$  at  $\overline{\overline{CP}}_1$  = "L" or on the negative going edge of  $\overline{CP}_1$  at  $\overline{CP}_0$  = "H". MR input of the "H" level resets counter to  $\overline{OO}_0$  = "H" and  $\overline{OO}_1$  ~  $\overline{OO}_7$  = "L" regardless of  $\overline{CP}_0$  and  $\overline{CP}_1$ .

The MN4022B/S are equivalent to MOTOROLA MC14022B and RCA CD4022B.

### Truth Table

MR	CP <sub>0</sub>	$\overline{\overline{CP}}_1$	Mode
Н	×	×	$O_0 = \overline{O}_{4-7} = H$ , $O_1 \sim O_7 = L$
L	Н	_	Counter Advance
L		L	Counter Advance
L	L	×	
L	×	Н	No Chausa
L	Н		No Change
L	_	L	





### **Maximum Ratings** $(Ta=25^{\circ}C)$

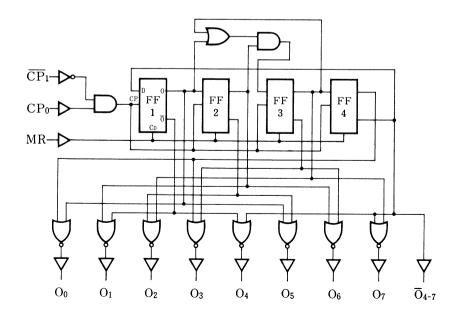
Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	Λ,
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	m W
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	re	Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
O :- + P	5				_	20		20		150	
Quiescent Power Supply Current	10	$I_{\mathrm{DD}}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$		40	_	40		300	μA
	15					80		80		600	
	5		$V_1 = V_{SS}$ or	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	VDD	_	0.05	_	0.05		0.05	V
Do W Do voi	15		$ 10  < 1\mu A$			0.05	_	0.05		0.05	
	5		V <sub>I</sub> =V <sub>SS</sub> or,	17	4.95	_	4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_I - V_{SS} $ or, $ I_O  < 1 \mu A$	VDD	9.95		9.95		9.95		V
	15		$ 1_0  < 1 \mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4		4	
Y 37 - 14	5			Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5		
Input Voltage High Level	10	$V_{1H}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4 V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1	_	0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6	_	3		2.4	_	
	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36	-	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0$ or $10V$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V_1$	, $V_I$ =0 or 15 $V$	3.6	_	3	_	2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I = 0 \text{ or } 5V$	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pmI_I$	$V_1 = 0$ or 15	SV		0.3	_	0.3		1	μA

### ■ Logic Diagram



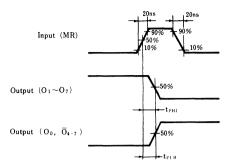


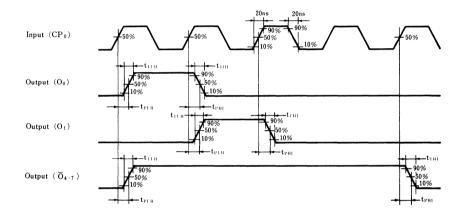
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5	1	_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
•	15	12.1		20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
-	15	1112	_	20	60	
	5		_	195	585	
Propagation Delay Time	10	tPHL		75	225	ns
$CP_0, \overline{CP}_1 \rightarrow On (H \rightarrow L)$	15	-1112	_	50	150	
	5		_	245	735	
Propagation Delay Time	10	t <sub>PLH</sub>	_	95	285	ns
$CP_0, \overline{CP}_1 \rightarrow On (L \rightarrow H)$	15	- Lii	_	60	180	
	5			245	735	<u> </u>
Propagation Delay Time	10	t <sub>PHL</sub>	_	90	270	ns
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7} (H \rightarrow L)$	15	1	_	60	180	
	5		_	190	570	<b>†</b>
Propagation Delay Time	10	t <sub>PLH</sub>	_	75	225	ns
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7} (L \rightarrow H)$	15	-12.1	_	50	150	
	5		_	130	390	
Propagation Delay Time	10	t <sub>PHL</sub>	_	55	165	ns
$MR \rightarrow O_1$ to $O_7$ $(H \rightarrow L)$	15	11112	_	40	120	
	5			130	390	
Propagation Delay Time MR→O <sub>0</sub> (L→H)	10	t <sub>PLH</sub>	_	55	165	ns
	15	1 211	_	40	120	
	5			110	330	
Propagation Delay Time	10	t <sub>PLH</sub>	_	45	135	ns
$MR \rightarrow \overline{O}_{4-7} (L \rightarrow H)$	15	1 2.1	_	35	105	
	5		_	70	210	
Hold Time	10	thold	_	25	75	ns
$CP_0 \rightarrow \overline{CP}_1$	15	-11014	_	15	45	
	5		<del> </del>	85	255	
Hold Time	10	thold	_	30	90	ns
$\overline{\mathrm{CP}}_1 \to \mathrm{CP}_0$	15		_	20	60	
	5	<b>†</b>	<del> </del>	35	105	
Minimum Clock Pulse Width	10	$t_{\text{WCP}}$	_	15	45	ns
	15	- "0"	_	10	30	
	5	1	_	35	105	
Minimum Reset Pulse Width	10	twmRH		15	45	ns
	15	T WINT	_	10	30	
	5		_	10	30	
Reset Recovery Time	10	t <sub>RMR</sub>	_	5	15	ns
	15	- K MK	_	5	15	
	5		3	6		1
Maximum Clock Frequency	10	fmax	8	16		ne
aximum Clock Frequency	15	ımax	12	24	_	ns
Input Capacitance	10	C <sub>I</sub>	12	4	7.5	pF

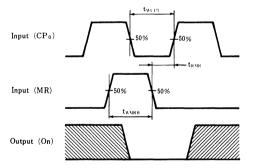
### 1. Switching Time Test Circuit

# 0 0 P.G. 2 MRC<sub>1</sub> -50pF

### 2. Waveforms





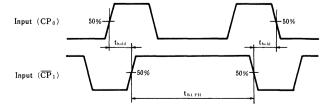


Waveforms showing recovery time for MR, minimum CP<sub>0</sub>

and MR pulse widths

Conditions:  $\overline{CP}_1$  = LOW while  $CP_0$  is triggered on a LOW to HIGH transition.

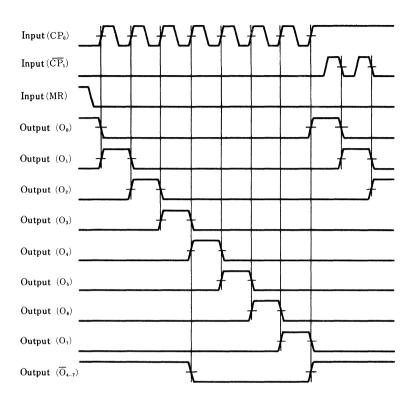
 $t_{WCP}$  and  $t_{RMR}$  also apply when  $CP_0$  = HIGH and  $\overline{CP}_1$  is triggered on a HIGH to LOW transition



Waveforms showing hold times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to Hold times are shown as positive values, but may be specified as negative values.



### Timing Diagram



# MN4023B/MN4023BS

### Triple 3-Input NAND Gates

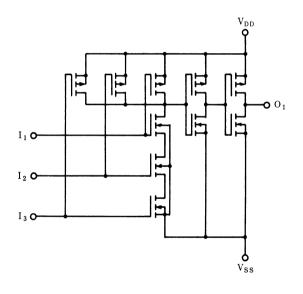
### Description

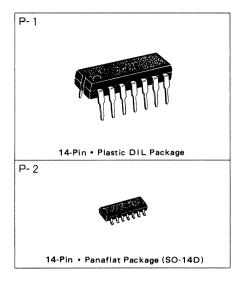
The MN4023B/S are positive 3-input NAND gates and have 3 circuits in a package.

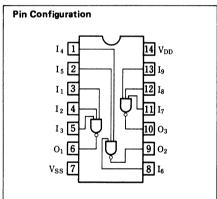
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4023B/S are equivalent to MOTOROLA MC14023B and RCA CD4023B.

### Schematic Diagram (1/3)







### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	-0.5~+18	V
Input Voltage	out Voltage		$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		± I,	max. 10	mA
Power Dissipation	Ta=-40~+60℃		max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	P <sub>D</sub>	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	r
Storage Temperatus	:e	Tstg	<del>-65</del> ∼+150	r

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V



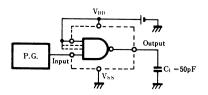
### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
ntem	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0 :	5				_	1		1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{ m DD}$		2		2		15	μA
outly continu	15					4		4	_	30	
	5		V-V	V		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	$V_{\mathrm{DD}}$		0.05		0.05		0.05	V
LOW LEVEL	15		$ I_0  < 1\mu A$		_	0.05	_	0.05		0.05	
_	5		37 — 37	V	4.95	_	4.95	_	4.95		
Output Voltage High Level	10	VoH		V DD	9.95		9.95	_	9.95	_	V
	15		$ I_{\rm O}  < 1\mu A$		14.95	_	14.95		14.95		
	5			Vo=0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3	_	3	_	3	V
Low Level	15		' "' '	V <sub>0</sub> =1.5V or 13.5V		4		4		4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			$\begin{array}{cccccccccccccccccccccccccccccccccccc$	_						
	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44	_	0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9	_	mA
25 25	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \text{V}$	3.6	_	3	_	2.4	_	
_	5		$V_0 = 4.6 V$	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9		mA
	15		$V_0 = 13.5 V$	$V_{I}=0 \text{ or } 15V$	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	5V	_	0.3		0.3		1	μA

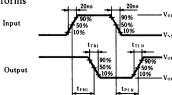
### **Switching Characteristics** $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15		_	20	. 60	
	5		_	65	195	
Propagation Delay Time	10	t <sub>PLH</sub>	_	30	90	ns
	15		_	25	75	
	5		_	65	195	
Propagation Delay Time	10	t <sub>PHL</sub>	_	25	75	ns
	15		_	15	45	
Input Capacitance		Cı	_		7.5	pF

### 1. Switching Time Test Circuit



2. Waveforms



# MN4024B/MN4024BS

### 7-Stage Binary Counters

### Description

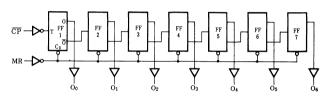
The MN4024B/S are 7-stage binary ripple counters composed of master-slave flip-flops.

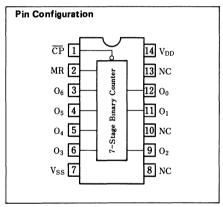
The counter advances on the negative going edge of the clock input. A High on the reset input (MR) clears all flip-flops and forces all outputs ( $O_0 \sim O_6$ ) Low, independent of the clock input.

The MN4024B/S are equivalent to MOTOROLA MC14024B and RCA CD4024B.

# P- 1 14-Pin • Plastic DIL Package P- 2 14-Pin • Panaflat Package (SO-14D)

### Logic Diagram





### Pin Explanation

 $\overline{\mathrm{CP}}$  : Clock input (  $\diagdown$  )

MR: Reset input

 $O_0 \sim O_6$ : Output (7 Bits)

### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW
(per package)	Ta=+60~+85°C	$P_D$	Decrease up to 200mW rating at 8mW/°C	m vv
Power Dissipation (	per output terminal)	P <sub>D</sub>	max. 100	mW
Operating Ambient Temperature		Topr	<b>−40~+85</b>	c
Storage Temperature		Tstg	-65~+150	C

<sup>\*</sup> VDD + 0.5V should be under 18V



### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	85℃	Unit
	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0	5					20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	v <sub>DD</sub> .	_	0.05		0.05	_	0.05	V
2011 2011	15		10  \ 1 \mu A			0.05	_	0.05	_	0.05	
	5		$V_I = V_{SS}$ or	V	4.95	********	4.95	Name	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1 \mu A$	VDD	9.95	-	9.95	Victorian	9.95		V
	15		10  \ 1μΑ		14.95		14.95	_	14.95		
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$		1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	VIL		Vo=1V or 9V		3	_	3		3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
F 77 14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5	-	3.5	1	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			Vo=1.5V or 13.5V	11	_	11	_	11	_	
_	5		$V_0=0.4V$	$V_I$ =0 or 5V	0.52	-	0.44	_	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0$ or $15V$	3.6		3		2.4		
_	5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5V	0.52	_	0.44		0.36	-	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9		mA
	15		$V_0 = 13.5 V$	$V_{I}=0 \text{ or } 15V$	3.6		3	-	2.4		
Output Current High Level	5	—Іон	$V_0 = 2.5V$	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_I$	$V_{\rm I} = 0 \text{ or } 15$	5V		0.3		0.3		1	μA

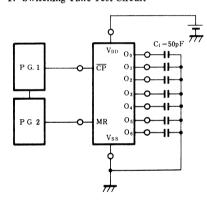
### 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5			60	180		
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns	
	15			20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns	
	15			20	60		
Propagation Delay Time	5			105	315		
<del>CP</del> →O <sub>0</sub> (L→H)	10	tPLH	_	45	135	ns	
CP→O <sub>0</sub> (L→H)	15			30	90		
Propagation Delay Time	5		_	100	300		
CP→O <sub>0</sub> (H→L)	10	tPHL	_	40	120	ns	
CF=00 (H=L)	15		_	25	75		
Propagation Delay Time	5		_	50	150		
On→On+1 (L→H)	10	t <sub>PLH</sub>	_	25	75	ns	
On→On+1 (L→H)	15		_	15	45		
Propagation Delay Time	5		_	60	180		
On→On+1 (H→L)	10	t <sub>PHL</sub>		25	75	ns	
On FORFI (II-L)	15		_	20	60		

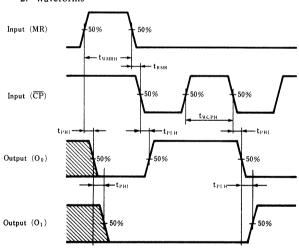
### ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$ (Continued)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	120	360	
MR→On (H→L)	10	t <sub>PHI</sub>		45	135	ns
MR→On (H→L)	15		_	30	90	
	5			30	90	
Minimum Clock Pulse Width	10	twcph		15	45	ns
	15			10	30	
	5			40	120	
Minimum Reset Pulse Width	10	twmrh		20	60	ns
	15			15	45	
	5			10	30	
Reset Recovery Time	10	t <sub>RMR</sub>		5	20	ns
	15			5	20	
	5		5	10		
Maximum Clock Frequency	10	fmax	13	25		ns
	15		18	35	_	
Input Capacitance		C <sub>I</sub>		-	7.5	pF

### 1. Switching Time Test Circuit



### 2. Waveforms



Waveforms showing propagation delays for MR to  $O_n$  and  $\overline{CP}$  to  $O_0$  , minimum MR and  $\overline{CP}$  pulse widths and recovery time for MR



# MN4025B/MN4025BS

### Triple 3-Input NOR Gates

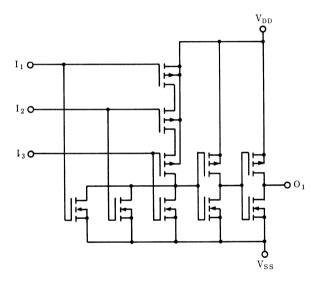
### Description

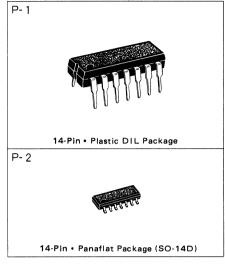
The MN4025B/S are positive 3-input NOR gates and have 3 circuits in a package.

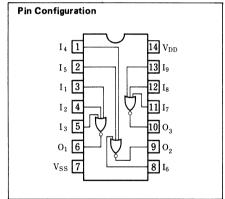
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increase of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4025B/S are equivalent to MOTOROLA MC14025B and RCA CD4025B.

### Schematic Diagram (1/3)







### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vi	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	-0.5~ V <sub>DD</sub> +0.5*	V
Peak Input · Output	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	<b>−40~+85</b>	${}^{\mathbb{C}}$
Storage Temperatur	re	Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

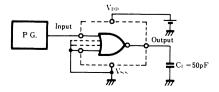
### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

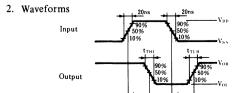
74	$V_{\mathrm{DD}}$	Sym-		G		-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Unit
0 :	5					1	_	1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{\rm I} = V_{\rm SS}  \text{or}  V_{\rm DD}$		2	_	2	_	15	μA
	15					4		4		30	
	5		$V_I = V_{SS}$ or	V		0.05	-	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1\mu$ A	VDD		0.05	_	0.05	_	0.05	V
2011 2011	15		10  < 1µA		_	0.05		0.05		0.05	
0	5		$V_I = V_{SS}$ or	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	VoH	$ I_0  < 1\mu A$	V DD	9.95	_	9.95	_	9.95	_	V
	15		10  \ 1μΛ		14.95		14.95		14.95	_	
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Y4 37-14	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5	_	3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4 V$	$V_I = 0$ or $5V$	0.52		0.44	_	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0=0.5V$	$V_I = 0$ or $10V$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4	_	
_	5		$V_0 = 4.6 V$	$V_I$ =0 or 5V	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3		1.1	_	0.9	_	mA
-	15		$V_0 = 13.5V$	$V_{I}=0 \text{ or } 15V$	3.6	_	3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0=2.5V$	$V_I$ =0 or 5V	1.7	_	1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	5V		0.3		0.3		1	μA

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_{L}\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left(\mathbf{V}\right)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		-	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
	5			60	180	
Propagation Delay Time	10	t <sub>Pl H</sub>	_	25	75	ns
	15			15	45	
	5		_	70	210	
Propagation Delay Time	10	t <sub>PHI</sub>	-	25	75	ns
	15			20	60	
Input Capacitance		$C_1$	_		7.5	pF







# MN4027B/MN4027BS

### Dual J-K Flip-Flops

### Description

The MN4027B/S are dual J-K flip-flops. Each flip-flop has independent J, K, set, clear and clock inputs and complementary outputs  $(0, \overline{0})$ .

For the J-K mode, both logic levels of clear and set are Low and the information is transferred to the output on the positive going edge of the clock pulse according to the state of J and K.

These are equivalent to MOTOROLA MC14027B and RCA CD4027B.

### Truth Table

		Input			Ou	tput
Sp	Съ	CP	J	K	$O_{n+1}$	$\overline{O}_{n+1}$
L	L		L	L	no cl	nange
L	L		Н	L	Н	L
L	L		L	Н	L	Н
L	L		Н	Н	$\overline{\mathrm{O}}_{\mathrm{n}}$	On
Н	L	×	×	×	Н	L
L	Н	×	×	×	L	Н
Н	Н	×	×	×	Н	Н
L	L	~	×	×	no cl	nange

Note) X: don't care

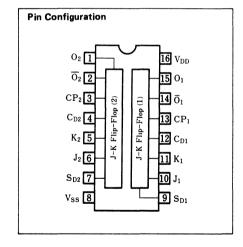
### Pin Explanation

J, K: Synchronous input CP: Clock input (\_\_\_\_\_)

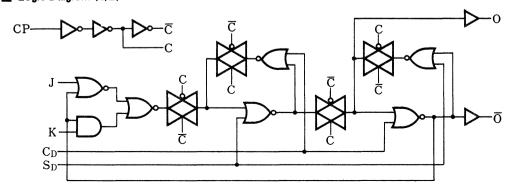
 $S_D$ : Asynchronous set direct input  $C_D$ : Asynchronous clear direct input

 $O, \overline{O}$ : Output

# 16-Pin • Panaflat Package (SO-16D)



### Logic Diagram (1/2)



### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	Λ.
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	1.
Output Voltage		$V_0$	$-0.5 \sim V_{DD} + 0.5^*$	Λ.
Peak Input · Output	t Current	± I <sub>1</sub>	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	11.
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW.
Power Dissipation (	per output terminal)	P <sub>D</sub>	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	$-65 \sim +150$	$^{\circ}$

<sup>\*</sup>V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{\rm SS} \! = \! 0V)$

	$V_{ m DD}$	Sym-		1:4:	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	T I
Item	(V)	bol	Conditions		min.	max.	min.	max.	mın.	max	Unit
	5				4	_	4		30		
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS} \text{ or } V_{DD}$			8		8	_	60	$\mu A$
	15			. 35		16		16		120	
_	5		37 – 37	17	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{i}=V_{ss}$ or	$V_{\mathrm{DD}}$	_	0.05	-	0.05		0.05	V
Dow Dove.	15		$ I_{\rm O}  < 1\mu A$		_	0.05	_	0.05		0.05	
0	5		V V	<b>\'</b> 7	4.95		4.95	_	4.95		
Output Voltage High Level	10	Von	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	V DD	9.95	_	9.95		9.95		V
	15		$ 10  < 1\mu A$		14.95		14.95		14.95	_	
	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	_	3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4		4	
T 4 37 14	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	-	7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36	-	
Output Current Low Level	10	Ioi	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	wanten	1.1	_	0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6		3		2.4	_	
	5		$V_0 = 4.6V$ ,	V <sub>i</sub> =0 or 5V	0.52		0.44		0.36		
Output Current High Level	10	—I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_i = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5V$	, $V_l$ =0 or 15 $V$	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_1$	$V_l = 0$ or 15	SV		0.3	_	0.3		1	μA



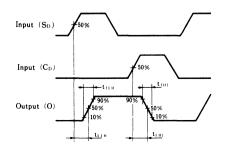
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15	1	_	20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
D	5		_	115	345	
Propagation Delay Time	10	t <sub>PLH</sub>		50	150	ns
$(CP \rightarrow O, \overline{O}) (H \rightarrow L)$	15			35	105	
D D. T.	5			115	345	
Propagation Delay Time	10	tpHL	_	50	150	ns
$(CP \rightarrow O, \overline{O}) (L \rightarrow H)$	15			35	105	
D. C. D.L. Time	5			75	225	
Propagation Delay Time	10	tPLH		35	105	ns
$(S_0 \rightarrow 0)$	15		_	25	75	
Proposition Delay Time	5			130	390	
Propagation Delay Time	10	t <sub>PHL</sub>		50	150	ns
$(C_D \rightarrow O)$	15			35	105	
	5		-	50	150	4
Minimum Set-up Time	10	tsu		15	45	ns
(J, K→CP)	15			10	30	
	5			40	120	
Minimum Clear Pulse Width Minimum Preset Pulse Width	10	twsDH	_	20	60	ns
Manualli i i eset i uise wiutii	15	twcDH	_	15	45	
	5		3	6	_	
Maximum Clock Frequency	10	fmax	7	15	_	MHz
	15		11	22	_	
Input Capacitance		Cı	_	_	7.5	pF

### • Switching Time Test Circuit

Test No.	J	K	$C_D$	$S_D$	CP
1	Н	Н	L	L	P.G.1
2	Н	Н	P.G. 1	P.G. 2	Н
3	P.G. 1	P.G. 1	L	L	P.G. 2

Note: P.G. = Pulse Generator

Test No. 2 Waveforms



Test No. 1 Waveforms  $\begin{array}{c} 20ns \\ \hline \\ Input \ (CP) \\ \hline \\ Output \ (O) \\ \end{array}$ 

Test No. 3 Waveforms

# MN4028B/MN4028BS

BCD-to-Decimal / Binary-to-Octal Decoders

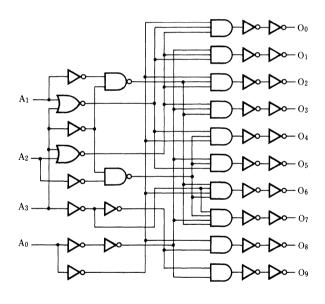
### Description

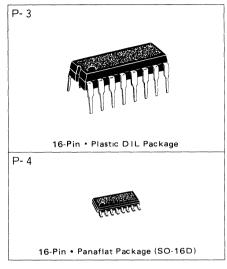
The MN4028B/S are 4-bit BCD-to-decimal decoders. A BCD code applied to inputs  $A_0$  through  $A_2$  causes the selected output  $(O_0 \sim O_9)$  to be High, the other nine remain Low.

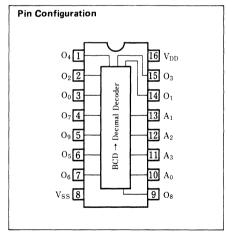
This may be used as a 1-OF-8 decoder with active low enable input for  $A_3$ .

The MN4028B/S are equivalent to MOTOROLA MC14028B and RCA CD4028B.

### Logic Diagram







### Pin Explanation

 $A_0{\sim}\,A_3$  : Output, 1-2-4-8BCD

 $O_0 \sim O_9$ : Address input

### Truth Table

	Inp	ut						Out	put				
A <sub>3</sub>	$A_2$	$A_1$	$A_0$	$O_0$	$O_1$	$O_2$	$O_3$	O <sub>4</sub>	O <sub>5</sub>	$O_6$	$O_7$	O <sub>8</sub>	$O_9$
L	L	L	L	Н	L	L	L	L	L	L	L	L	L
L	L	L	Н	L	Н	L	L	L	L	L	L	L	L
L	L	Н	L	L	L	Н	L	L	L	L	L	L	L
L	L	Н	Н	L	L	L	Н	L	L	L	L	L	L
L	Н	L	L	L	L	L	L	Н	L	L	L	L	L
L	Н	L	Н	L	L	L	L	L	Н	L	L	L	L
L	Н	Н	L	L	L	L	L	L	L	Н	L	L	L
L	Н	Н	Н	L	L	L	L	L	L	L	Н	L	L
Н	L	L	L	L	L	L	L	L	L	L	L	Н	L
Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н
Н	L	Н	L	L	L	L	L	L	L	L	L	Н	L
Н	L	Н	Н	L	L	L	L	L	L	L	L	Ĺ	Н
Н	Н	L	L	L	L	L	L	L	L	L	L	Н	L
Н	Н	L	Н	L	L	L	L	L	L	L	L	L	Н
Н	Н	Н	L	L	L	L	L	L	L	L	L	Н	L
Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	Н

### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$ m V_{DD}$	-0.5∼+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	±Ιι	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal		$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient	Temperature	Topr	$-40\!\sim\!+85$	°C
Storage Temperatur	·e	Tstg	$-65 \sim +150$	C

<sup>\*</sup>V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{ m DD}$	Sym-	Conditions	Ta=-	−40°C	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
nem	(V)	bol	Collations	min.	max.	min.	max.	min.	max.	Onit
	5				20		20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or $V_{DD}$		40		40		300	$\mu$ A
Supply Cultent	15				80	_	80		600	
**************************************	5		V-V		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or $V_{\rm DD}$ $ I_{\rm O}  < 1\mu{\rm A}$		0.05		0.05		0.05	V
	15		$ 10  < 1 \mu A$		0.05		0.05		0.05	
	5		V-V	4.95		4.95		4.95		
Output Voltage High Level	10	VoH	$V_{\rm I} = V_{\rm SS}$ or $V_{\rm DD}$ $ I_{\rm O}  < 1\mu{\rm A}$	9.95		9.95		9.95		V
	15		10  < 1 µA	14.95		14.95		14.95		

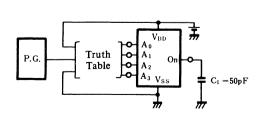
### ■ DC Characteristics (V<sub>SS</sub>=0V) (continued)

14	$V_{DD}$	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
Item	(V)	bol		onditions	min.	max.	min.	max.	min.	max.	Unit
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1 \mu A$	Vo=1V or 9V	_	3	_	3	_	3	v
	15			V <sub>0</sub> =1.5V or 13.5V		4		4	_	4	
T	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	_	3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7	_	7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11	_	11		
0 0	5		$V_0=0.4V$	$V_l = 0 \text{ or } 5V$	0.52	_	0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15V	3.6	_	3		2.4		
0	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36	_	
Output Current High Level	10	—Іон	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3	_	1.1	_	0.9		mA
	15			, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	— I <sub>OH</sub>	$V_0=2.5V$ ,	$V_I$ =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	SV	_	0.3	_	0.3		1	μA

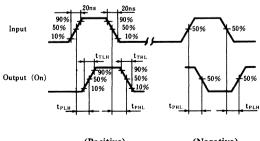
### **Switching Characteristics** $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	mın.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
	5		_	100	300	
Propagation Delay Time	10	tplH	_	45	135	ns
	15		_	30	90	
	5		_	110	330	
Propagation Delay Time	10	tPHL	_	50	150	ns
	15			35	105	
Input Capacitance		Cı		_	7.5	pF

### 1. Switching Time Test Circuit



### 2. Waveforms



(Positive)

(Negative)

# MN4029B/MN4029BS

### 4-Bit Presettable Up/Down Counters

### Description

The MN4029B/S are synchronous up/down counters which can be used for either binary or decade counting.

An appropriate value of the counter is presettable by setting data inputs  $(P_0 \sim P_3)$  while the load input is High.

The counter advances on the positive going edge of the clock input when the  $\overline{\text{CE}}$  and PL are Low.

The selection of binary or decade is determined by  $BIN/\overline{DEC}$  input (High level is binary, Low level is decade) and Up or Down counter depends on  $UP/\overline{DN}$  input (up at High level, down at Low level).

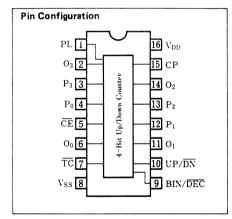
These are equivalent to MOTOROLA MC14029B and RCA CD4029B.

# P- 3 16-Pin • Plastic DIL Package P- 4 16-Pin • Panaflat Package (SO-16D)

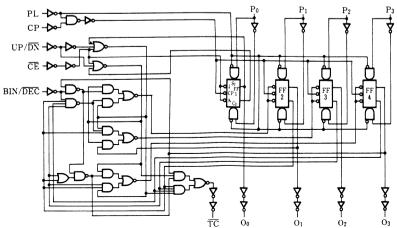
### Pin Explanation

 $P_0 \sim P_3$ : Data input (4 Bits)  $O_0 \sim O_3$ : Output (4 Bits) CP : Clock input ( $\checkmark$ ) PL : Load input

 $\begin{array}{c} \overline{CE} & : \ Enable \ input \\ UP/\overline{DN} & : \ Up/down \ input \\ BIN/\overline{DEC} : \ Binary/decade \ input \end{array}$ 



### Logic Diagram



### ■ Truth Table

PL	BIN/DEC	UP/DN	CE	CP	Mode
Н	×	×	×	×	parallel load
L	×	×	Н	×	no change
L	L	L	L		count-down
L	L	Н	L		count-up
L	Н	L	L		count-down, binary
L	Н	Н	L		count-up, binary

Note) X: don't care

### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{ m DD}$	-0.5~+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Outpu	ak Input · Output Current		max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	11/	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (per output terminal)		$P_D$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	$^{\circ}$	
Storage Temperatur	e	Tstg	-65~+150	°C	

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS} {=} 0V)$

	$V_{DD}$	Sym-			Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	
Item	$(\mathbf{v})$	bol	,	Conditions	min.	max.	min.	max.	min.	max.	Unit
O : + P	5					20		20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_I = V_{SS}$ or $V_{DD}$		40	_	40		300	μA
	15					80	_	80	_	600	
	5		V=V= or	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ $ I_0  < 1 \mu A$	$V_{\rm I} = V_{\rm SS} \text{ or } V_{\rm DD}$		0.05		0.05	_	0.05	V
	15		10  < 1 mA			0.05		0.05		0.05	
0	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$				9.95		9.95	-	V
	15		101 < 1 μ21		14.95		14.95		14.95	_	
T X7. 14	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
Input Voltage	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5	_	3.5		
High Level	10	VIH	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7	_	7	_	7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
Outroot Comment	5		$V_0=0.4V$	$V_I$ =0 or 5 $V$	0.52	_	0.44	_	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0=0.5V$	$V_I$ =0 or 10V	1.3	_	1.1	_	0.9		mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Outmut Command	5		$V_0 = 4.6V$	$V_I = 0$ or $5V$	0.52		0.44	_	0.36	-	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$	$V_I$ =0 or 10V	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	SV .		0.3		0.3		1	μA

**Switching Characteristics**  $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$ 

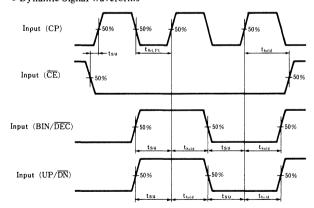
Switching Characteristics  Item		V <sub>SS</sub> =0V, (	min.	typ.	max,	Unit
nem	V <sub>DD</sub> (V)	Symbol	111111.	<del></del>		Ullit
Out and Direction	5	1	_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15	-		20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15	ļ	<del>-</del>	20	60	
Propagation Delay Time	5		_	145	435	
CP→On (H→L)	10	t <sub>PHL</sub>	_	55	165	ns
	15			40	120	
Propagation Delay Time	5		_	160	480	
CP→On (L→H)	10	t <sub>PLH</sub>	_	60	180	ns
Of Foli (E Fil)	15			40	120	
Propagation Delay Time	5		_	280	840	
CP→TC (H→L)	10	tPHL	_	105	315	ns
CF TC (H TL)	15			70	210	
Propagation Delay Time	5		_	195	585	
$CP \rightarrow \overline{TC} (L \rightarrow H)$	10	t <sub>PLH</sub>	_	75	225	ns
CP→TC (L→H)	15			55	165	
Droposotion Delay Time	5			120	360	
Propagation Delay Time	10	t <sub>PHL</sub>	_	50	150	ns
PL→On (H→L)	15		_	35	105	
	5			170	510	
Propagation Delay Time	10	t <sub>PLH</sub>		65	195	ns
$PL \rightarrow On (L \rightarrow H)$	15	1.211	MAN PM	45	135	
	5		_	180	540	
Propagation Delay Time	10	tPHL		70	210	ns
$\overline{CE} \rightarrow \overline{TC} \ (H \rightarrow L)$	15	VERE		50	150	
	5			170	510	
Propagation Delay Time	10	t <sub>PLH</sub>	_	65	195	ns
$\overline{CE} \rightarrow \overline{TC} (L \rightarrow H)$	15	tPLH .	_	50	150	115
	5	-		55	165	
Minimum Clock Pulse Width	10			20	60	
Millimum Clock Fulse width	1	twcpl		1		ns
	15	<del> </del>		15	45	
Minimum DY Dulas W/1441	5		_	80	240	
Minimum PL Pulse Width	10	twPLH		25	75	ns
	15			15	45	ļ
DI D	5		_	75	225	
PL Recovery Time	10	t <sub>RPL</sub>	-	25	75	ns
	15			20	60	
Set-up Time	5		_	135	405	
BIN/ <del>DEC</del> →CP	10	tsu	_	45	135	ns
	15			30	90	
Set-up Time	5		_	150	450	
UP/ <del>DN</del> →CP	10	tsu	_	55	165	ns
OI / DIV -OI	15		-	35	105	

## Switching Characteristics (Ta = 25%, $V_{SS} = 0V$ , $C_L = 50pF$ ) (continued)

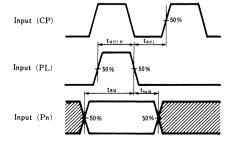
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
Cat up Time	5		-	60	180		
Set-up Time $\overline{CE} \rightarrow CP$	10	tsu		25	75	ns	
CE→CP	15		_	20	60		
Set-up Time	5			35	105		
Pn→PL	10	tsu	_	10	30	ns	
F∏→FL	15		_	5	15		
II-14 Time	5		_	- 90	45		
Hold Time BIN/DEC→CP	10	thold		- 30	15	ns	
BIN/DEC→CF	15		_	- 20	10		
Hold Time	5		_	-135	15		
UP/DN→CP	10	thold	_	- 50	0	ns	
UP/DN→CP	15			- 35	-5		
Hold Time	5		_	- 30	30		
<del>CE</del> →CP	10	thold	_	- 10	10	ns	
CE-CF	15		_	- 10	5		
	5		_	- 20	15		
Hold Time Pn→PL	10	thold	_	- 10	0	ns	
rn→r∟	15		_	- 5	0		
	5		4	8	_		
Maximum Clock Frequency	10	fmax	12	25		MHz	
	15		18	35	_		
Input Capacitance		Cı	_	_	7.5	pF	

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### • Dynamic Signal Waveforms

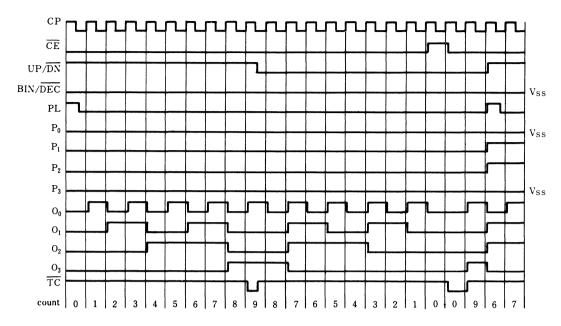


Waveforms showing minimum pulse width for CP, set-up and hold times for CE to CP, BINI/DEC to CP and UP/DN to CP, set up and hold times are shown as positive values but may be specified as negative values.

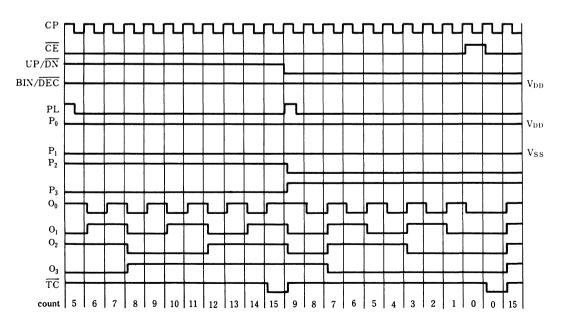


Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P $_{\rm h}$  to PL, set up and hold times are shown as positive values but may be specified as negative values.

### ■ Timing Diagrams



Decade:  $(P_0 = L, P_3 = L, BIN/\overline{DEC} = L)$ 



Binary:  $P_0 = H$ ,  $P_1 = L$ ,  $BIN/\widehat{DEC} = H$ 

# MN4030B/S, MN4070B/S

### Quad Exclusive-OR Gates

### Description

The MN4030B/S and MN4070B/S are EXCLUSIVE-OR gates and have 4 circuits in a package.

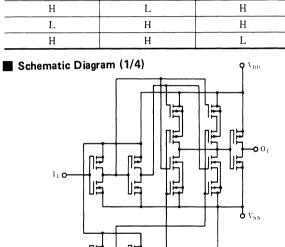
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

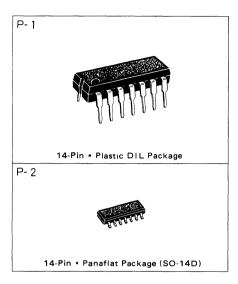
Typical applications include digital comparators and parity

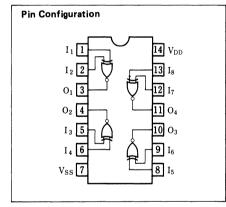
These are equivalent to MOTOROLA MC14070B and RCA CD4070B.

### Truth Table

I <sub>1</sub>	I <sub>2</sub>	O <sub>1</sub>
L	L	L
Н	L	Н
L	Н	Н
Н	Н	L







### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V	
Input Voltage		VI	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage	put Voltage		$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Outpu	t Current	$\pm I_1$	max. 10	mA	
Power Dissipation	Ta=-40~+60°C	D	max. 400	mW	
(per package)	Ta=+60~+85℃	$P_{\rm D}$	Decrease up to 200mW rating at 8mW/°C		
Power Dissipation (per output terminal)		P <sub>D</sub>	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

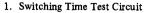
<sup>\*</sup> VDD + 0.5V should be under 18V

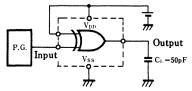
### $\blacksquare$ DC Characteristics $(V_{\rm SS}{=}0V)$

Item	$V_{DD}$	Sym-			Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	T. T *A
Item	(V)	bol	C	onditions	min.	max.	min.	max.	min.	max.	Unit
0: 10	5				_	1		1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2		2		15	μA
Surpry Carrent	15					4		4	-	30	
	5		$V_I = V_{SS}$ or	37		0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	V <sub>DD</sub>		0.05	-	0.05		0.05	V
Low Devel	15		1 <sub>0</sub>   < 1 µA			0.05		0.05		0.05	
	5		V-V	17	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_{\rm O}  < 1\mu A$	=V <sub>SS</sub> or V <sub>DD</sub>			9.95		9.95	_	V
	15		10  < 1µA		14.95	_	14.95	_	14.95	-	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	V <sub>IL</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4.	_	4	
Y 4 X7 14	5			3.5		3.5		3.5			
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11	_	
_	5		$V_0=0.4V$	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I$ =0 or 10V	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6V$	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10 $V$	1.3		1.1		0.9		mA
22.01	15		Vo=13.5V	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV .		0.3		0.3	*****	1	μA

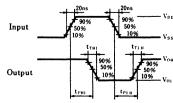
## $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		_	60	180		
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns	
	15			20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>		30	90	ns	
	15			20	60		
	5		_	75	225		
Propagation Delay Time	10	tplH		30	90	ns	
	15			25	75		
	5			85	255		
Propagation Delay Time	10	t <sub>PHL</sub>		35	105	ns	
	15			30	90		
Input Capacitance		Cı	_	_	7.5	pF	





### 2. Waveforms



# MN4035B/MN4035BS

### 4-Bit Universal Shift Registers

### Description

The MN4035B/S are edge-triggered 4-bit shift registers with both serial and parallel inputs.

Data is loaded into the register from parallel inputs when parallel enable is High or from serial JK inputs when it is Low and data is shifted one position on the positive going edge of the clock input.

The outputs are non-inverting when the  $T/\overline{C}$  input is High and inverting when the  $T/\overline{C}$  input is Low. A High on the MR input resets all registers, independent of any other input conditions.

These are equivalent to MC14035B and RCA CD4035B.

### Truth Table

Serial Action (First Stage)

	Inp	ut		Output	Mode
СР	J	$\overline{K}$	MR	$O_0$	Mode
	Н	Н	L	Н	D Glin Glan
	L	L	L	L	D flip-flop
	Н	L	L	$\overline{O}_0$	toggle
	L	Н	L	O <sub>0</sub>	no change
×	×	×	Н	L	reset

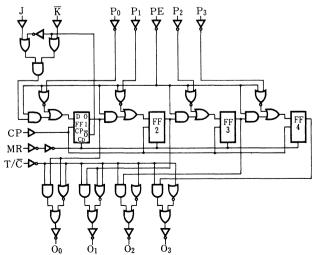
Note) T/C = H, PE = L

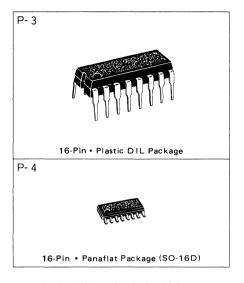
Parallel Action

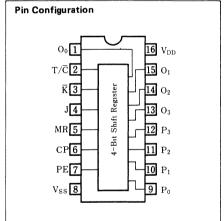
СР	Input				Output			
	$P_0$	P <sub>1</sub>	P <sub>2</sub>	$P_3$	$O_0$	O <sub>1</sub>	O <sub>2</sub>	$O_3$
$\overline{\mathcal{L}}$	Н	Н	Н	Н	Н	Н	Н	Н
	L	L	L	L	L	L	L	L

Note)  $T/\overline{C} = H$ , RE = H, MR = L

### Logic Diagram







### Pin Explanation

 $P_0 \sim P_3$ : Data input  $O_0 \sim O_3$ : Output CP: Clock input MR: Reset input PE: Enable input

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
nput Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}{=}0V)$

	$V_{\mathrm{DD}}$	Sym-		11.1	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	<b>85℃</b>	
Item	(V)	bol	(	Conditions	min.	max.	min.	max.	min.	max.	Unit
Onderson Design	5				_	20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I} = V_{SS}$ or $V_{DD}$		_	40	_	40		300	μA
	15				80	_	80	-	600		
_	5		V <sub>i</sub> =V <sub>ss</sub> or	V		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1 \mu A$	V <sub>DD</sub>	_	0.05	_	0.05	-	0.05	V
Low Level	15		$ 1_0  < 1 \mu A$			0.05	_	0.05	-	0.05	
	5		V — V	17	4.95		4.95		4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	VDD	9.95		9.95		9.95	_	V
	15		$ 1_0  < 1 \mu A$		14.95		14.95		14.95		
	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$	_	3	_	3	_	3	V
20.1. 20.101	15			$V_0 = 1.5 V \text{ or } 13.5 V$	_	4	_	4	_	4	
T	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7	_	7		v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11	_	
	5		$V_0 = 0.4 V$	$V_i = 0$ or $5V$	0.52	_	0.44	-	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I{=}0 \ or \ 10\mathrm{V}$	1.3	_	1.1	_	0.9		mA
Low Lover	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6	_	3	_	2.4		
_	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I{=}0\ \mathrm{or}\ 10\mathrm{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>i</sub> =0 or 15	SV		0.3		0.3		1	μA

# $\blacksquare$ Switching Characteristics $(Ta\!=\!25^{\circ}\!C\,,~V_{SS}\!=\!0\,V,~C_{L}\!=\!50pF)$

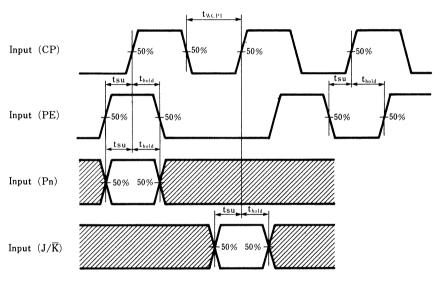
Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	$t_{TLH}$	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15		_	20	60	
	5		_	170	510	
Propagation Delay Time	10	tPHL		70	210	ns
$CP \rightarrow On (H \rightarrow L)$	15			50	150	
	5		_	150	450	
Propagation Delay Time	10	t <sub>Pl H</sub>		65	195	ns
$CP \rightarrow On (L \rightarrow H)$	15		_	45	135	
	5			175	525	
Propagation Delay Time	10	t <sub>PHI</sub>		70	210	ns
$MR \rightarrow On (H \rightarrow L)$	15	-1111		50	150	
****	5			160	480	
Propagation Delay Time	10	t <sub>Pl H</sub>		65	195	ns
$MR \rightarrow On (L \rightarrow H)$	15	or in	_	45	135	
	5			115	345	
Propagation Delay Time	10	t <sub>PHI</sub>		55	165	ns
$T/\overline{\mathbb{C}} \rightarrow On \ (H \rightarrow L)$	15	or mr	_	40	120	
	5	<del> </del>		110	330	
Propagation Delay Time	10	t <sub>PLH</sub>		50	150	ns
$T/\overline{C} \rightarrow On \ (L \rightarrow H)$	15	CP1.H	_	35	105	
	5	<del> </del>		45	135	
Minimum Clock Pulse Width	10	twoPL		20	60	ns
	15	CWCPL		15	45	
	5	<del> </del>	_	30	90	
Minimum Reset Pulse Width	10	twmrh		15	45	ns
	15	CWMRH	_	10	30	
	5	+		55	165	
Reset Recovery Time	10	$t_{RMR}$		20	60	ns
Reset Receivery Tame	15	CRMR		15	45	
	5			105	315	
Set-up Time	10	tsu	- Market	40	120	ns
Pn→CP	15	tsu	_	25	75	113
	5	<del> </del>		100	300	
Set-up Time	10	tsu		40	120	ns
PE→CP	15	LSu	_	25	75	113
	5			105	315	
Set-up Time	10	tsu		40	120	ns
J, K→CP	15	LSu	_	25	75	,13
	5	<del>                                     </del>	<del> </del>	10	35	
Hold Time	10	thold		10	30	ns
Pn→CP	15	-noid	_	10	30	
	1 10	1	1	10	1 00	1



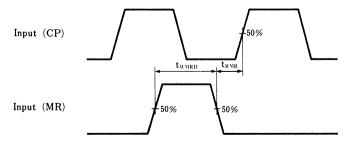
### Switching Characteristics $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
II 11 T	5		Martiner	-5	30	
Hold Time PE→CP	10	thold		-5	20	ns
1 12-01	15			-5	10	
Hold Time	5			-5	20	
Hold Time J, K→CP	10	thold		0	20	ns
J, K-Cr	15			0	20	
	5		5	10		
Maximum Clock Frequency	10	fmax	12	25		MHz
	15		18	35		
Input Capacitance		$C_{I}$	_		7.5	pF

#### • Dynamic Signal Waveforms



Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.



Waveforms showing minimum MR pulse width and MR recovery time.

# MN4040B/MN4040BS

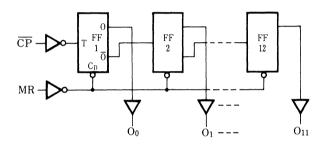
P- 3

# 12-Stage Binary Counters

#### Description

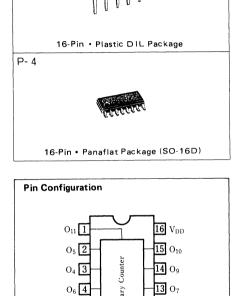
The MN4040B/S are 12-stage binary ripple counters with a clock input. The reset input and outputs are fully buffered. The counter advances on the negative going edge of the clock input. A High on the MR input clears all counter stages and forces all outputs ( $O_0 \sim O_{11}$ ) Low, independent of the clock input. These are suitable for frequency dividers and center-control circuits, and are equivalent to MOTOROLA MC14040B and RCA CD4040B.

#### Logic Diagram



#### Pin Explanation

 $O_0 \sim O_{11}$ : Output (12 Bits)



 $12 O_8$ 

11 MR

10 CP

#### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_1$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C		
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

\* VDD + 0.5V should be under 18V



# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

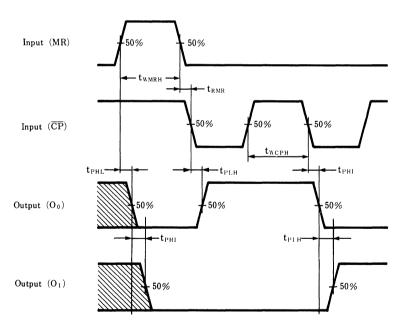
Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
ntem	(V)	bol		onditions	min.	max.	min.	max.	min.	max.	Unit
	5				-	20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>l</sub> =V <sub>SS</sub> or	$V_{DD}$		40	_	40		300	μA
0 P P V	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1\mu$ A	VDD		0.05		0.05		0.05	V
Low Level	15		$ 1_0  < 1\mu A$		_	0.05	_	0.05	_	0.05	
	5		V - V	17	4.95		4.95	_	4.95	-	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu \text{A}$	$V_{ m DD}$	9.95		9.95	_	9.95		V
	15		$ 1_0  < 1 \mu A$		14.95		14.95		14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3		3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4		4		4	
* . ** 1.	5			Vo=0.5V or 4.5V	3.5	-	3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11		11	_	
	5		$V_0 = 0.4V$	$V_1 = 0$ or $5V$	0.52	-	0.44	_	0.36		
Output Current Low Level	10	IoL	$V_0=0.5V$	$V_I {=} 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6	-	3	_	2.4		
	5		$V_0 = 4.6 V$	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36		
Output Current High Level	10	-Іон	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	-	1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4	-	
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	$\pmI_{I}$	$V_1 = 0 \text{ or } 15$	SV		0.3		0.3	_	1	μA

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Propagation Delay Time  CP→O₀ (L→H)	5		_	105	315	
	10	$t_{ m PLH}$	_	50	150	ns
	15		_	35	105	
Propagation Delay Time	5		_	105	315	
$\overline{CP} \rightarrow O_0  (H \rightarrow L)$	10	t <sub>PHL</sub>	_	45	135	ns
	15	Ì	_	30	90	
Propagation Delay Time	5			70	210	
On $\rightarrow$ On $+1$ (L $\rightarrow$ H)	10	t <sub>PLH</sub>	_	25	75	ns
$On \rightarrow On + 1  (L \rightarrow H)$	15			20	60	
Propagation Delay Time	5		_	80	240	
	10	t <sub>PHL</sub>	_	30	90	ns
$On \rightarrow On_{+1}  (H \rightarrow L)$	15			20	60	

 $\blacksquare$  Switching Characteristics  $(Ta\!=\!25\%\,,~V_{\rm SS}\!=\!0\,V,~C_{\rm L}\!=\!50pF)$ 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5			180	540	
MR→On (H→L)	10	t <sub>PHL</sub>		90	270	ns
MR-On (H-L)	15	ļ	_	70	210	
	5		_	25	75	
Minimum Clock Pulse Width	10	twcph		15	45	ns
	15		_	10	30	
	5			65	195	
Minimum Reset Pulse Width	10	twmRH	_	50	150	ns
	15		_	45	135	
	5		_	60	180	
Reset Recovery Time	10	$t_{ m RMR}$	_	35	105	ns
	15			25	75	
	5		5	10	_	
Maximum Clock Frequency	10	fmax	13	25	_	MHz
	15		18	35	_	
Input Capacitance		C <sub>I</sub>	_	_	7.5	pF

#### • Dynamic Signal Waveforms



Waveforms showing propagation delays for MR to  $O_n$  and  $\overline{CP}$  to  $O_0$ , minimum MR and  $\overline{CP}$  pulse widths and recovery time for MR



# MN4042B/MN4042BS

### Quad D Latches

#### Description

The MN4042B/S are quad D latches which have a common clock line and different data input terminals.

When the input (El) is " $\hat{H}$ " level, the output (O) shows the input (D) while input (E<sub>0</sub>) is on the positive going edge; when the input (E<sub>0</sub>) is on the negative going edge, output (O) maintains the input (D).

When the input  $(E_0)$  is on the negative going edge, the output (D) does not change even if input (D) changes.

When input (E<sub>1</sub>) is at the "L" level, input (D) appears on the output (O) while input (E<sub>0</sub>) is at the "L" level, and while input (E<sub>0</sub>) is at the "H" level, Latch operates.

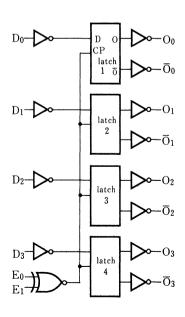
The MN4042B/S are equivalent to MOTOROLA MC14042B and RCA CD4042B.

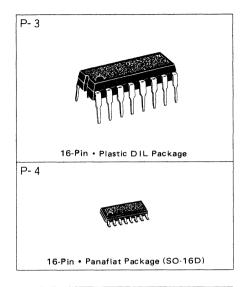
#### Tructh Table

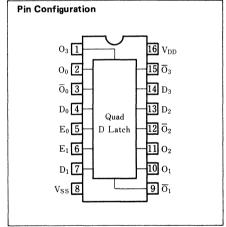
Inp	ut	Output				
E <sub>0</sub>	E <sub>1</sub>	0				
L	L	D				
L	Н	latch				
Н	L	latch				
Н	Н	D				

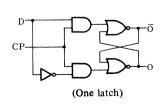
#### Logic Diagram

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Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	$-0.5 \sim +18$	V
Input Voltage		$V_{\rm I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm\mathrm{I}_{\mathrm{I}}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	מ	max. 400	mW
(per package)	Ta=+60~+85℃	$\dot{\mathbf{P}}_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	m vv
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	<b>−40~+85</b>	°C
Storage Temperature		Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

#### **DC** Characteristics (V<sub>SS</sub>=0V)

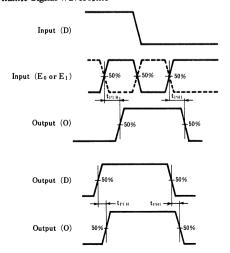
Item	$V_{DD}$	Sym-	(	Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Omt
Ouiescent Power	5				-	4		4	_	30	
Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	8		8	_	60	μA
	15					16		16		120	
	5		V-V on	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol		$V_1 = V_{SS} \text{ or } V_{DD}$		0.05		0.05		0.05	V
1:			$ I_0  < 1\mu A$		_	0.05	_	0.05		0.05	
0	5		$V_I = V_{SS}$ or	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	V DD	9.95		9.95		9.95		V
	15		$ 1_0  \sim 1 \mu R$		14.95		14.95		14.95	_	
	5			Vo=0.5V or 4.5V		1.5	_	1.5	-	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Y XY . 14	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11		
	5		$V_0 = 0.4 V$	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0=0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1	_	0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6	_	3		2.4		
	5		$V_0 = 4.6V$ ,	$V_I = 0$ or $5V$	0.52		0.44	-	0.36		
Output Current High Level	10	—I <sub>он</sub>	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	—Іон	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	5V	_	0.3		0.3		1	μA



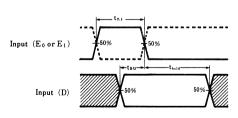
■ Switching Characteristics (Ta=25°C,  $V_{SS}=0$ V,  $C_L=50$ pF)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	-	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Proposition Deley Time	5			95	285	
Propagation Delay Time $D \rightarrow O$ , $\overline{O}$ $(H \rightarrow L)$	10	$t_{ exttt{PHL}}$		40	120	ns
	15		_	30	90	
D D.1	5			85	255	
Propagation Delay Time $D \rightarrow O$ , $\overline{O}$ $(L \rightarrow H)$	10	t <sub>PLH</sub>		40	120	ns
	15			30	90	
	5			130	390	
Propagation Delay Time	10	tpHL	ann manns	50	150	ns
$E \rightarrow O, \overline{O} (H \rightarrow L)$	15		_	35	105	
December D. 1. Ti	5			120	360	
Propagation Delay Time	10	tplH		50	150	ns
$E \rightarrow O$ , $\overline{O}$ $(L \rightarrow H)$	15			35	105	
	5		_	45	135	
Minimum Enable Pulse Width	10	$t_{ m WE}$		20	60	ns
	15			15	45	
G	5		_	10	30	
Set-up Time	10	tsu	_	5	20	ns
D→E	15			5	20	
II-14 Tim-	5		_	-5	15	
Hold Time	10	thold	_	0	15	ns
D→E	15		_	0	15	
Input Capacitance		Ci	_	_	7.5	pF

#### • Dynamic Signal Waveforms



Waveforms showing propagation delays for D to O, with latch enabled  $\,$ 



Waveforms showing minimum enable pulse width, set-up time and hold time for E and D

Satury and hold-times are shown as positive values but may

Set-up and hold-times are shown as positive values but may be specified as negative values.

# MN4043B/MN4043BS

# Quad R/S Latches

#### Description

The MN4043B/S are latches composed of quad independent R/S flip-flop.

They are suitable for 4-bit data processing due to the combination of NOR gates.

Four outputs can be high impedance by the common input (EO) = L regardless of latch contents, and can easily be connected to the bus line.

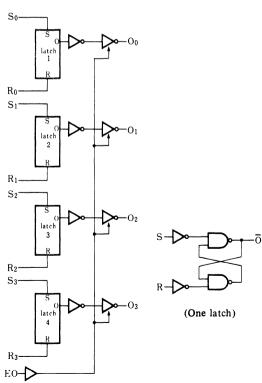
The MN4043B/S are equivalent to MOTOROLA MC14043B and RCA CD4043B.

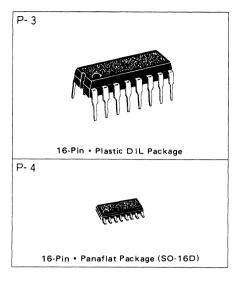
#### Tructh Table

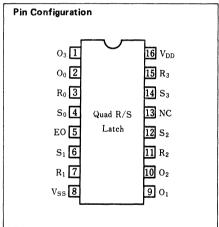
	Input					
	S	R	0			
L	×	×	Z			
Н	L	Н	L			
Н	Н	×	Н			
Н	L	L	latch			

Note) X: don't care Z: high impedance

#### Logic Diagram







Ite	m	Symbol	Ratings	Unit		
Supply Voltage		$V_{ m DD}$	-0.5~+18	V		
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V		
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V		
Peak Input · Output Current		$\pm I_1$	max. 10	mA		
Power Dissipation	Ta=-40~+60℃	D	max. 400			
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW.		
Power Dissipation (	Power Dissipation (per output terminal)		max. 100	mW		
Operating Ambient	perating Ambient Temperature Topr -40~+85			°C		
Storage Temperatur	e	Tstg	-65~+150	°C		

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

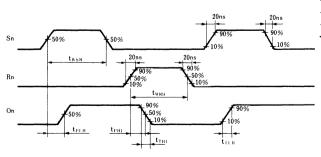
# $\blacksquare$ DC Characteristics $(V_{SS}{=}0V)$

	Onuractoristic	$V_{DD}$	Sym-			Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	
	Item	(V)	bol	(	Conditions	min.	max.	min.	max.	min.	max.	Unit
0	D	5				_	4	_	4		30	
	ent Power Current	10	$I_{DD}$	$V_{I}=V_{SS}$ or	$V_{DD}$		8		8	_	60	μA
		15					16		16	_	120	
_		5		37 37	17	-	0.05		0.05		0.05	
Output Low L	t Voltage evel	10 V <sub>o</sub>		$V_{\rm I} = V_{\rm SS}$ or	$V_{\mathrm{DD}}$		0.05		0.05	_	0.05	V
		15		$ I_0  < 1\mu A$			0.05	_	0.05		0.05	
		5		V-V	17	4.95		4.95		4.95		
Outpu High L	t Voltage evel	10	V <sub>OH</sub>	$V_I = V_{SS} \text{ or } V_{DD}$ $ I_O  < 1\mu A$		9.95	_	9.95		9.95	_	V
		15		$ 10  < 1\mu A$		14.95		14.95		14.95		
_	Y \$7-14	5			Vo=0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	_	3	V	
	15			V <sub>0</sub> =1.5V or 13.5V	_	4	_	4		4		
	17 1.	5			Vo=0.5V or 4.5V	3.5	enumen.	3.5		3.5		
Input High L	Voltage .evel	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	entrantum.	v
		15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11	_	
_	_	5		$V_0 = 0.4V$	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Outpu Low L	t Current evel	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0$ or $10V$	1.3	_	1.1		0.9		mA
20 2		15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15V	3.6	_	3		2.4		
		5		$V_0 = 4.6V$	$V_I$ =0 or 5 $V$	0.52		0.44		0.36	_	
Outpu High L	t Current Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
		15		$V_0 = 13.5 V$	$V_{I}=0 \text{ or } 15V$	3.6		3		2.4		
Output (	Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$	$V_I = 0 \text{ or } 5 \text{ V}$	1.7	_	1.4	_	1.1	_	mA
Input Le	eakage Current	15	$\pm I_I$	$V_i = 0 \text{ or } 15$	SV		0.3	_	0.3		1	μA
3-State	Leakage Current High Level	15	I <sub>ozh</sub>	$V_0 = V_{DD}$			1.6	_	1.6		12	μA
Output Pin	Leakage Current Low Level	15	-I <sub>ozL</sub>	$V_0 = V_{SS}$			1.6		1.6	_	12	μΑ

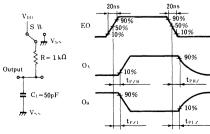
# 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	mın.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THI</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5			90	270	
Rn→On (H→L)	10	t <sub>PHL</sub>		35	105	ns
Kn→On (H→L)	15			25	75	
Propagation Delay Time	5		_	65	195	
	10	tPLH		25	75	ns
$Sn \rightarrow On (L \rightarrow H)$	15		_	15	45	
High Level Output Disable Time	5			45	135	
EO→On (H)	10	$t_{ m PHZ}$	_	20	60	ns
	15		_	10	30	
Low Level Output Disable Time	5			50	150	
EO→On (L)	10	t <sub>PLZ</sub>	_	20	60	ns
EO→On (L)	15			10	30	
High Land Output Enghle Time	5		_	25	75	
High Level Output Enable Time   EO→On (H)	10	t <sub>PZH</sub>		15	45	ns
EO→On (H)	15		_	10	30	
Low Level Output Enable Time	5		_	40	120	
EO→On (L)	10	t <sub>PZL</sub>	_	20	60	ns
EO→On (L)	15		_	15	45	
	5		_	15	45	
Low Level Minimum Sn Pulse Width	10	twsH		10	30	ns
	15		_	8	24	
	5		_	15	45	
Low Level Minimum Rn Pulse Width	10	twan	_	10	30	ns
W Marit	15		_	8	24	
Input Capacitance		Cı	-	_	7.5	pF

### • Dynamic Signal Waveforms



Item	S	R	S W	C
t <sub>PH7</sub>	$V_{DD}$	$V_{SS}$	V <sub>SS</sub>	A
tplz	V <sub>ss</sub>	$V_{DD}$	$V_{DD}$	В
t <sub>PZH</sub>	V <sub>DD</sub>	Vss	Vss	A
1021	Vec	Vnn	Vpp	E





# MN4044B/MN4044BS

# Quad R/S Latches

#### Description

The MN4044B/S have built-in quad independent R/S flip-flops. They are suitable for 4-bit data processing due to the combination of NAND gates.

Four outputs can be high impedance by common input (EO) = L regardless of the latch contents.

These are equivalent to MOTOROLA MC14044 and RCA CD4044B.

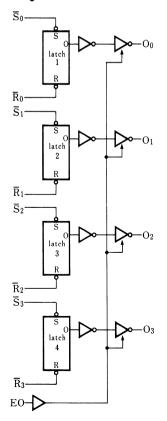
#### ■ Truth Table

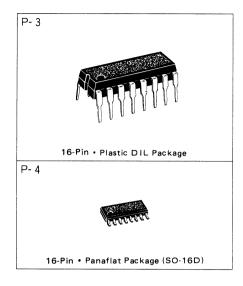
	Input			
EO	S	R	0	
L	×	×	Z	
Н	L	Н	Н	
Н	×	L	L	
Н	Н	Н	latch	

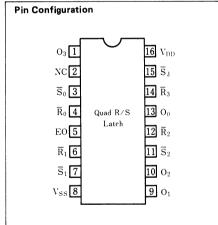
Note) X: don't care

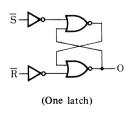
Z: high impedance

#### Logic Diagram









# $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{o}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	$^{\circ}$ C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

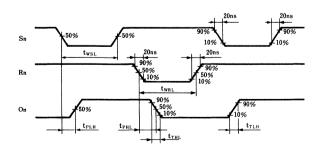
Item	V <sub>DD</sub>	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Onn
Ouisses n	5				_	4	_	4	_	30	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{DD}$		8		8		60	μA
	15				_	16	_	16		120	
	5		$V_{i}=V_{ssor}$	V	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1\mu$ A	$\mathbf{v}_{\mathrm{DD}}$		0.05	_	0.05		0.05	V
	15		$ 1_0  < 1\mu A$			0.05	_	0.05		0.05	
	5		$V_I = V_{SSOT}$	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_I - V_{SS}$ or $ I_O  < 1\mu$ A	V DD	9.95	_	9.95		9.95		V
	15		10  < 1µA		14.95		14.95		14.95		
Input Voltage Low Level	5			$V_0 = 0.5 V \text{ or } 4.5 V$	_	1.5		1.5	_	1.5	
	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	-	4		4		4	
7 77 1.	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$	11		11		11		
_	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_I$ =0 or 10V	1.3		1.1	_	0.9	_	mA
20.1. 20.1.	15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15V	3.6	_	3	_	2.4		
_	5		$V_0 = 4.6V$	V <sub>I</sub> =0 or 5V	0.52		0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6	_	3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$	$V_I = 0 \text{ or } 5 \text{ V}$	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	$V_I = 0 \text{ or } 15$	SV	_	0.3		0.3	_	1	μA
3-State Leakage Current High Leve	15	I <sub>ozh</sub>	$V_0 = V_{DD}$			1.6		1.6		12	
Output Pin Leakage Current Low Leve	15	$-I_{OZL}$	$V_0 = V_{SS}$			1.6		1.6	_	12	μA



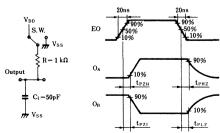
### Switching Characteristics $(Ta = 25^{\circ}C, V_{SS} = 0V, C_{L} = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Propagation Delay Time	5			90	270	
• •	10	t <sub>PHL</sub>	_	40	120	ns
$\overline{R}n \rightarrow On \ (H \rightarrow L)$	15			30	90	
Danas action Deleas Time	5			90	270	
Propagation Delay Time	10	t <sub>PLH</sub>	_	40	120	ns
$\overline{S}n \rightarrow On \ (L \rightarrow H)$	15			30	90	
High Level Output Disable Time	5		-	50	150	
EO→On (H)	10	t <sub>PHZ</sub>		30	90	ns
	15			25	75	
T 10	5			30	90	
Low Level Output Disable Time	10	t <sub>PLZ</sub>		25	75	ns
EO→On (L)	15			20	60	
Itiah Lavel Outroot Frankla Time	5			50	150	
High Level Output Enable Time	10	t <sub>PZH</sub>		25	75	ns
EO→On (H)	15			20	60	
I am I aval Outmut Enghla Tima	5			50	150	
Low Level Output Enable Time EO→On (L)	10	$t_{PZL}$		25	75	ns
EO→On (L)	15			20	60	
	5		45	15	_	
Low Level Minimum Sn Pulse Width	10	twsL	30	10	_	ns
	15		24	8		
	5		45	15		
Low Level Minimum Rn Pulse Width	10	twrL	30	10	_	ns
11 100/11	15		24	8	_	
Input Capacitance		Cı		_	7.5	pF

#### • Dynamic Signal Waveforms



Item	S	R	SW.	C
tPHZ	V <sub>DD</sub>	Vss	V <sub>ss</sub>	A
t <sub>PL7</sub>	Vss	$V_{DD}$	$V_{DD}$	В
tpzH	V <sub>DD</sub>	V <sub>ss</sub>	V <sub>SS</sub>	A
tezi	Vee	V <sub>DD</sub>	Von	E



# MN4046B/MN4046BS

# Phase-Locked Loops

#### Description

This MN4046B/S are phase-locked loop circuits composed of two phase comparators, VCO, source follower and zener diode. The two comparators have common signal inputs  $SIGN_{{\bf IN}}$  and

COMP<sub>IN</sub>.

 ${\rm SIGN_{IN}}$  should be used by directly connecting to large voltage signals or by connecting small voltage signal through serial capacitors.

Small voltage signals are adjusted to the linear area of the amplifier by the self-bias circuit.

Phase comparator 1 is an Exclusive-OR gate which outputs digital error signal  $PC1_{OUT},$  and shifts phase by  $90^\circ$  with the central frequency between  $SIGN_{\mbox{\footnotesize{IN}}}$  signal and  $COMP_{\mbox{\footnotesize{IN}}}$  signal (50% duty cycle)

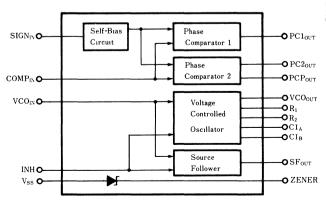
Phase comparator 2 outputs digital error signals  $PC_{OUT}$  and  $PCP_{OUT}$  and phase shifts between  $SIGN_{IN}$  and  $COMP_{IN}$  (duty cycle is arbitrary) is  $0^{\circ}$ .

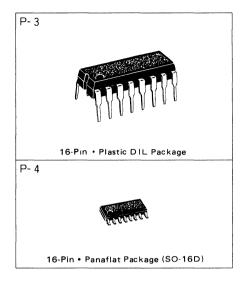
The frequency of signal VCO $_{OUT}$  obtained by the linear VCO is defined by the voltage of input VCO $_{IN}$  and the constant of the resistor and capacitor connected to  $R_1,\,R_2,\,C_{1A}$  and  $C_{1B}$ .

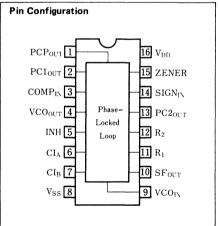
When  $VOC_{IN}$  signal is necessary and there is no space for loading, source follower output  $SF_{OUT}$  together with an external resistor is used. When inhibit input INH is "1" level, stand-by power dissipation can be minimized because the VCO and source follower are disabled.

A zener diode should be used to adjust the power supply source. The MN4046B/S can be widely used for modulation and demodulation of FM and FSK, composition and discrimination of frequencies, tone decoding, synchronization and adjustment of data, and conversion of voltage and frequencies.

#### Block Diagram









Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage	nput Voltage		-0.5~V <sub>pD</sub> +0.5*	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	ver Dissipation (per output terminal) P <sub>D</sub>		max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	re e	Tstg	<del>-65~+150</del>	$^{\circ}$

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{\rm SS}\!=\!0V)$

	$V_{\mathrm{DD}}$	Sym-			Ta=-	- <b>40</b> ℃	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	
Item	(V)	bol	(	Conditions	min.	max.	min.	max.	min.	max.	Unit
0 :	5				_	20		20		150	
Quiescent Power Supply Current	10	$I_{DD}$	INH = H,	$SIGN_{IN} = H$	_	40		40		300	$\mu$ A
Supply Culton	15				_	80		80		600	
	5		37 37	37	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	V <sub>DD</sub>	_	0.05		0.05		0.05	V
	15		$ I_0  < 1\mu A$		_	0.05		0.05		0.05	
	5		37 37	***	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	VoH	$V_{\rm I} = V_{\rm SS}$ or	$V_{ m DD}$	9.95		9.95		9.95	_	V
Ingh Bever	15		$ I_0  < 1\mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	_	3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4		4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	_	3.5	_	
Input Voltage High Level	10	VIH	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11	_	
	5		$V_0 = 0.4V$ ,	V <sub>i</sub> =0 or 5V	0.52	_	0.44		0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3	_	1.1		0.9		mA
Do W Devel	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
_	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9	_	mA
11.6.1 20 101	15		$V_0 = 13.5 V$	$V_{\rm I}=0$ or $15\rm V$	3.6		3	_	2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	$V_I$ =0 or 5 $V$	1.7	_	1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	5V		0.3		0.3		1	μA
Input Capacitance		$C_{I}$						7.5			pF

#### ■ Electrical Characteristics

### $\bullet$ Switching Characteristics $(Ta\!=\!25^{\circ}\!\!\!\mathrm{C}\,,\ V_{SS}\!=\!0\,V,\ C_{L}\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	Condition	min.	typ.	max.	Unit
	5			_	60	180	
Output Rise Time	10	tTLH		_	30	90	ns
	15			_	20	60	
Output Fall Time	5			_	60	180	
	10	t <sub>THL</sub>		materia	30	90	ns
	15			_	20	60	

#### • Phase · Comparator

Item		$V_{DD}(V)$	Symbol	Condition	min.	typ.	max.	Unit
		5			_	750	_	
Input Resistance	SIGNIN	10	D			220	_	1.0
input itesistance		15	$R_{IN}$			140		kΩ
	COMPIN	15			_			
		5		AC Couple-SIGN <sub>IN</sub>	_	150	_	
Minimum Input Sens	itivity	10	$V_{IN}$	$R_1 = 10k\Omega$ , $R_2 = \infty$		150		mV <sub>PP</sub>
		15		$C_I = 100pF$	_	200		
DOG 1 MOV	COMP	5			_		1.5	
DC Couple-SIGN <sub>IN</sub> : Low Level	COMPIN	10	VIL		_		3	V
_		15				_	4	
DC Couple-SIGN <sub>IN</sub> : COMP <sub>IN</sub> High Level		5			3.5		_	
		10	$V_{IH}$		7	_	_	V
		15			11	_		

### Voltage Control Oscillator

Item	$V_{DD}(V)$	Symbol	Condition	min.	typ.	max.	Unit
	5		$VCO_{IN} = V_{DD}$	0.5	1	_	
Maximum Frequency	10	fmax	$R_1 = 10k\Omega$ , $R_2 = \infty$	1	2		MHz
	15		$C_1 = 50pF$	1.3	2.7	_	
Temperature-Frequency Stability	5			_	0.12	_	
	10		$R_2 = \infty$	_	0.04	_	%/℃
23	15			_	0.015	_	
	5		$VCO_{IN} = 2.50V \pm 0.30V R_1 > 10k \Omega$	_	0.50	_	
Linearity	10		$R_2 = \infty$ $VCO_{IN} = 5.00V \pm 2.50V \\ R_1 > 400k \Omega$	1 —	0.25	_	%
	15		$\frac{\text{VCO}_{\text{IN}}}{\text{R}_1 = 1 \text{M}\Omega} = 7.50 \text{V} \pm 5.00 \text{V}$	-	0.25	_	
Output Duty Cycle	5 ~ 15	δ			50	_	%
Input Resistance (VCO <sub>IN</sub> )	5 ~ 15	$R_{IN}$		_	10 <sup>6</sup>	_	МΩ

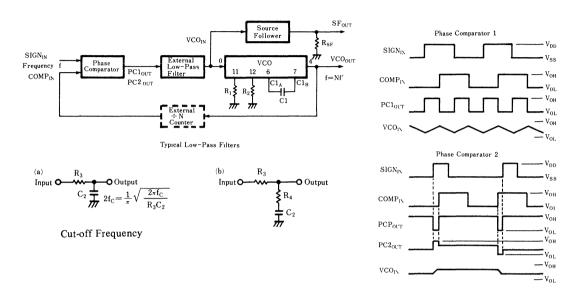
#### • Source · Follower

Item	$V_{DD}(V)$	Symbol	ol Condition		typ.	max.	Unit
	5		VCO <sub>IN</sub> -SF <sub>OUT</sub>	_	1.5	-	
Offset Voltage	10		$R_{SF} = 50k\Omega$	_	1.7	_	V
	15		$R_{SF} = 50R4I$	_	1.8	_	
	5		$VCO_{IN}\!=\!2.50V\!\pm\!0.30V$ , $R_{SF}\!>\!\!50k\Omega$	_	0.3		
Linearity	10		$VCO_{IN}\!=\!5.00V\pm\!2.50V$ , $R_{SF}\!>\!50k\Omega$		1.0		%
	15		$VCO_{IN} = 7.50V \pm 5.00V$ , $R_{SF} > 50k\Omega$		1.3	_	

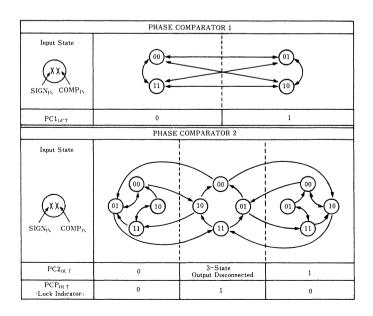
#### Zener Diode

Item	$V_{DD}(V)$	Symbol	Condition	min.	typ.	max.	Unit
Zener Voltage		Vz	$I_Z = 50 \mu A$		7.3		V
Action Resistance		Rz	$I_Z = 1 \text{ mA}$	_	25		Ω

(Fig. 1) General PLL Connections



(Fig. 2) Phase · Comparator Mode Diagrams



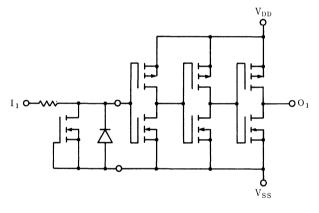
# MN4049B/MN4049BS

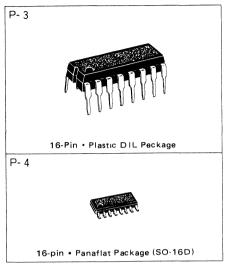
# Hex Inverting Buffers

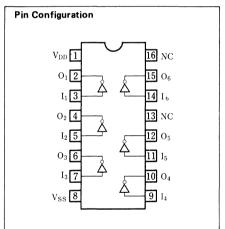
#### Description

The MN4049B/S are hex inverting buffers and can be used to convert the logic level. These devices provide high output current to drive TTLs and DTL directly, and are used as CMOS-to-TTL converters with two normal-TTL drive capability. They have good switching characteristics due to triple inverting circuits. The MN4049B/S are equivalent to MOTOROLA MC14049B and RCA CD4049B.

#### ■ Schematic Diagram (1/6) & Input Protection Circuit







# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
nput Voltage		Vi	-0.5~+18	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	k Input · Output Current		max. 40	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	137
(per package)	Ta=+60~+85℃	$\mathbf{P}_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatus	re e	Tstg	$-65 \sim +150$	C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

### ■ Guaranteed Fan-Out for Logic Circuit Series

Drive IC	Guaranteed Fan-Out
Normal TTL	2
74LS	9
74L	16

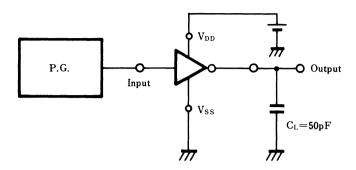
# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

T4	$V_{\mathrm{DD}}$	Sym-			Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol		onditions	min.	max.	min.	max.	min.	max.	Unit
Online of P	5					4	_	4		30	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or $V_{DD}$		_	8		8	_	60	μA
	15				-	16	_	16		120	
5			V-V	X7	_	0.05	_	0.05	- Allendaria	0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or $ I_O  < 1\mu A$	v <sub>DD</sub>		0.05		0.05		0.05	V
	15		$ 1_0  < 1\mu A$			0.05	_	0.05	_	0.05	
Ontant Walter	5		$V_I = V_{SS}$ or	V'	4.95		4.95	_	4.95	-	
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	<b>V</b> DD	9.95		9.95		9.95	-	V
	15		110  \ 1μΛ		14.95		14.95		14.95		
	5			$V_0 = 0.5 V \text{ or } 4.5 V$	_	1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$		3		3		3	V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$		4		4		4	
Immut Waltaga	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		v
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	$V_0=1V \text{ or } 9V$	7	_	7		7		
	15			$V_0 = 1.5 V \text{ or } 13.5 V$	11		11		11	_	
0.10.10.00.00	4.75		$V_0=0.4V$		3.5		2.9		2.3	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	12		10	_	8	_	mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	24		20		16	_	
Outros Comment	5		$V_0=4.6V$	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3	_	1.1	_	0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	$V_I$ =0 or 5 $V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_{\rm I} = 0 \text{ or } 15$	5V		0.3		0.3		1	μA

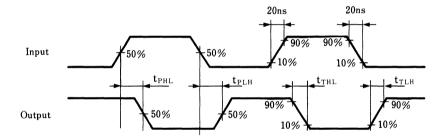
# $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_{L}\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left(\mathrm{V}\right)$	Symbol	min.	typ.	max.	Unit	
	5			60	180		
Output Rise Time	10	$t_{TLH}$	_	30	90	ns	
	15		_	20	60		
	5			25	75		
Output Fall Time	10	t <sub>THL</sub>		10	30	ns	
	15			7	21		
	5			60	180		
Propagation Delay Time	10	t <sub>PLH</sub>		30	90	ns	
	15		_	25	75		
	5			50	150		
Propagation Delay Time	10	$t_{ m PHL}$		20	60	ns	
	15		_	15	45		
Input Capacitance		Cı	_	<del>-</del>	7.5	pF	

# 1. Switching Time Test Circuit



#### 2. Waveforms





# MN4050B/MN4050BS

# Hex Non-Inverting Buffers

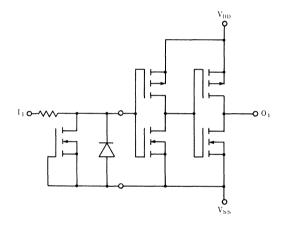
#### Description

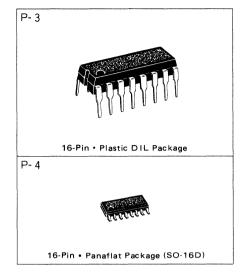
The MN4050B/S are hex non-inverting buffers which can be used to convert the logic level.

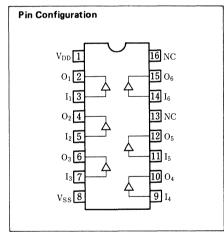
These devices provide high output current to drive TTLs and DTL directly, and are used as CMOS-to-TTL converters with two normal-TTL drive capability. They have good switching characteristics due to double inverting circuits.

The MN4050B/S are equivalent to MOTOROLA MC14050B and RCA CD4050B.

#### Schematic Diagram (1/6) & Input Protection Circuit







### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		$V_{\rm I}$	-0.5~+18	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	ak Input · Output Current		max. 40	mA
Power Dissipation	Ta=-40~+60℃	n	max. 400	
(per package)	Ta=+60~+85°C	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient Temperature To		Topr	-40~+85	°C
Storage Temperatur	re	Tstg	<del>-65</del> ∼+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

# ■ Guaranteed Fan-Out for Logic Circuit Series

Drive IC	Guaranteed Fan-Out
Normal TTL	2
74LS	9
74L	16

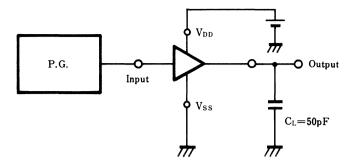
# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

T4	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25℃</b>	Ta=	<b>85</b> ℃	T	
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit	
0.1	5				_	4	_	4		30		
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	8		8		60	$\mu$ A	
	15					16		16	- 1	120		
	5		V-V	37	_	0.05	_	0.05	_	0.05		
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	$V_{\mathrm{DD}}$		0.05	_	0.05		0.05	V	
Low Level	15		$ I_{\rm O}  < 1\mu A$		_	0.05		0.05		0.05		
_	5		V - V	37	4.95		4.95	_	4.95			
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	V DD	9.95		9.95	_	9.95		V	
	15		$ 1_0  < 1\mu A$		14.95		14.95	_	14.95			
Input Voltage Low Level	5		$ I_{\rm O}  < 1\mu{\rm A}$	Vo=0.5V or 4.5V	_	1.5		1.5	_	1.5		
	10	$V_{IL}$		Vo=1V or 9V	_	3	_	3	_	3	V	
	15			Vo=1.5V or 13.5V		4		4	_	4		
	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		v	
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7	_	7	_	7			
	15			Vo=1.5V or 13.5V	11		11		11			
_	4.75		$V_0 = 0.4V$		3.5		2.9	_	2.3	_		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0$ or $10V$	12	_	10	_	8		mA	
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	24	_	20	_	16	_		
	5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5 $V$	0.52		0.44		0.36	_		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10 $V$	1.3		1.1		0.9	_	mA	
IIIGII LEVEI	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3	_	2.4	_		
Output Current High Leve!	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1	_	mA	
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV		0.3		0.3		1	μA	

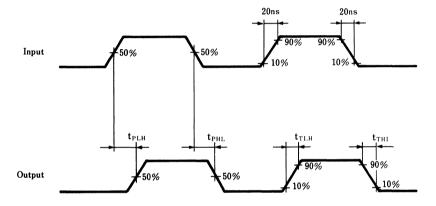
#### Switching Characteristics (Ta = 25%, $V_{SS} = 0V$ , $C_L = 50pF$ )

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		-	60	180		
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns	
	15		_	20	60		
Output Fall Time	5		_	25	75		
	10	t <sub>THL</sub>		10	30	ns	
	15		_	7	21	L	
	5		_	55	165	ns	
Propagation Delay Time	10	t <sub>PLH</sub>	_	25	75		
	15			20	60		
	5		-	35	105		
Propagation Delay Time	10	t <sub>PHL</sub>	_	20	60	ns	
	15		_	15	45		
Input Capacitance	4	Cı	_	_	7.5	pF	

# 1. Switching Time Test Circuit



#### 2. Waveforms



# MN4051B/MN4051BS

# 8-Channel Analog Multiplexers

#### Description

The MN4051B/S are analog multiplexer which control 8-channel analog switching by 3-input digital signals.

ON/OFF output voltage ratio is high and cross-talk between analog switches is low.

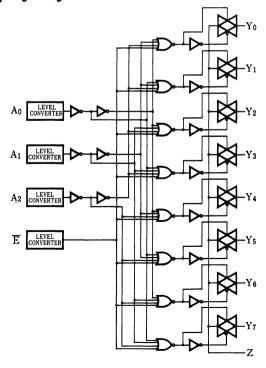
The MN4051B/S are equivalent to MOTOROLA MC14051B and RCA CD4051B.

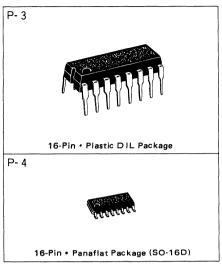
#### Truth Table

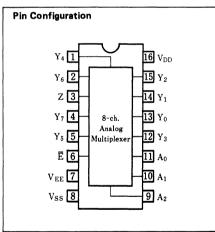
	Inp	ut		Channel
Ē	A <sub>2</sub>	$A_1$	$A_0$	ON
L	L	L	L	$Y_0-Z$
L	L	L	Н	$Y_1-Z$
L	L	Н	L	Y <sub>2</sub> -Z
L	L	Н	Н	$Y_3-Z$
Ĺ	Н	L	L	$Y_4-Z$
L	Н	L	Н	$Y_s-Z$
L	Н	Н	L	$Y_6 - Z$
L	Н	Н	Н	Y,-Z
Н	×	×	×	All OFF

Note) X: don't care

#### ■ Logic Diagram





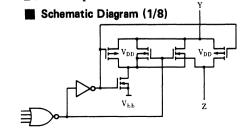


#### Pin Explanation

Y<sub>0</sub>~Y<sub>7</sub>: Analog input/output

 $A_0 \sim A_2$ : Address input Z: Common input/output

E: Enable input





Ite	m	Symbol	Ratings	Unit
Supply Voltage	Supply Voltage		-0.5∼+18	V
Input Voltage	Input Voltage		$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage Vo		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	11/
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	peroutput terminal)	P <sub>D</sub>	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	:e	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

•	$V_{DD}$	Sym-			Ta=-40℃		Ta=	25℃	Ta=85℃		Unit
Item	(V)	bol		Conditions		max.	min.	max.	min.	max.	Omt
O : P	5					20	_	20		150	
Quiescent Power Supply Current	10	$I_{\mathrm{DD}}$	$V_{I} = V_{SS}$ or	$V_{ m DD}$		40		40		300	μA
2.44.7	15					80		80		600	
5		Vo=0.5V or 4.5V		1.5		1.5		1.5			
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu$ A	Vo=1V or 9V		3		3		3	V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$		4		4		4	
Y	5			Vo=0.5V or 4.5V	3.5		3.5	_	3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	V <sub>I</sub> =0 or 15V		0.3		0.3		1	μA

Item	V <sub>DD</sub> — V <sub>EE</sub> (V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance 5		R <sub>on</sub>	$V_I=5V$		200	800	
	5		$V_I=2.5V$		550	1300	Ω
			$V_I = 0.25V$		200	800	
		Ron	$V_I = 10V$		80	300	
On Resistance	10		$V_I = 5V$		100	350	Ω
			$V_I = 0.25V$	_	80	300	
			$V_I = 15V$	promposed	60	200	
On Resistance	15	Ron	$V_i=7.5V$		80	250	Ω
			$V_1=0.25V$		60	200	

Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1)	5			_	15	45	
Vis→Vos (H→L)	10	t <sub>PHL</sub>	$R_{L}=10k\Omega$	-	5	15	ns
VIS-VOS (II-L)	15		$C_L = 50pF$	_	5	15	
Propagation Delay Time (Fig. 1)	5		$\overline{E} = V_{SS}$	_	15	45	
Vis→V <sub>os</sub> (L→H)	10	tPLH	E=Vss	_	5	15	ns
VIS-VOS (L-H)	15			_	5	15	
Propagation Delay Time (Fig. 1)	5				170	510	
Propagation Delay Time $\langle \cdot \cdot \cdot \rangle$ An $\rightarrow V_{OS}$ (H $\rightarrow$ L)	10	tPHL	$R_L = 10k\Omega$	-	65	195	ns
An Vos (n L)	15			-	50	150	
(Fig. 1)	5		$C_L = 50 pF$		160	480	
Propagation Delay Time (Fig. 1)	10	$t_{PLH}$	$\overline{E} = V_{SS}$		65	195	ns
$An \rightarrow V_{OS} (L \rightarrow H)$	15			_	45	135	
Output Disable Time (Fig. 1)	5			-	125	375	
	10	$t_{\mathrm{PHZ}}$	D 1010	_	90	270	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15		$R_L = 10k\Omega$	_	85	255	
- (Fig. 1)	5		$C_L = 50 pF$	_	155	465	
Output Disable Time (Fig. 1)	10	t <sub>PLZ</sub>	$\overline{E} = V_{DD}$	_	120	360	ns
$\overline{E} \rightarrow V_{OS}$ (L)	15			_	115	345	
/rt- +\	5			_	190	570	
Output Enable Time (Fig. 1)	10	t <sub>PZH</sub>	D 1010	_	75	225	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15	12	$R_L = 10k\Omega$	_	50	150	
(Ei- 1)	5		$C_L = 50 pF$	_	195	585	
Output Enable Time (Fig. 1)	10	tPZL	$\overline{E} = V_{DD}$		75	225	ns
$\overline{E} \rightarrow V_{OS}$ (L)	15	1122		_	50	150	
	5				0.25		<b></b>
Sine Wave Distortion (Fig. 2)	10		$R_L = 10 k\Omega$ , $C_L = 15 pF$	_	0.04	_	%
	15		$f_{is} = 1 \text{ kHz},  V_{is} = \frac{1}{2} V_{DD(P-P)}$		0.04		"
	5				_	_	
Crosstalk (Fig. 3)	10		$R_L = 1 k\Omega$	_	1	_	MHz
(Between 2 Channels)	15		$Vis = \frac{1}{2} V_{DD (P-P)}$	_			
	5			<u> </u>			
Crosstalk (Fig. 1)	10		$R_L=10k\Omega$ , $C_L=15pF$	_	50		mV
$(Address Input \rightarrow Output)$	15	ĺ	$\overline{E}$ or An= $V_{DD}$		_	_	***
	5			<b>-</b>			<u> </u>
Feedthrough (Fig. 2) (Note. 1)	10		$R_L = 1 k\Omega$ , $C_L = 5 pF$	l _	1		MHz
(OFF)	15		$Vis = \frac{1}{2} V_{DD (P-P)}$		_		WIIIZ
	5				13		
Propagation (Fig. 2) (Note. 2)	10		$R_L = 1 k\Omega$ , $C_L = 5 pF$	_	40		MHz
Frequency			$Vis = \frac{1}{2} V_{DD (P-P)}$		70		WIIIZ
Input Capacitance (Control)	15	Cı		<u> </u>		7.5	pF
Input Capacitance (Switch)		Cı			10	1.3	pF
Input cupucitation (S. Hell)		<u> </u>	L.		10	L	hr.

Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

 $A_0$   $A_1$   $A_2$  E  $C_L$ 

Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit

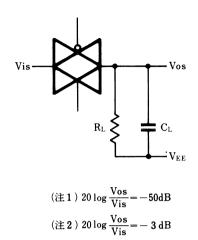
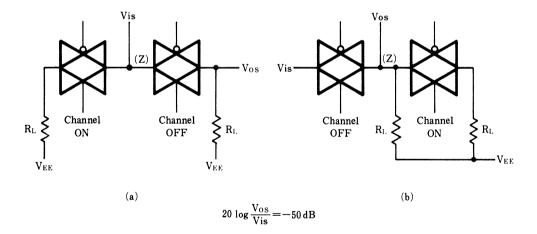


Fig. 3 Crosstalk Test Circuit



# MN4052B/MN4052BS

# Dual 4-Channel Analog Multiplexers

#### Description

The MN4052B/S are dual 4-channel analog multiplexer/demultiplexers which enable selection of digital or analog signals and their complexes.

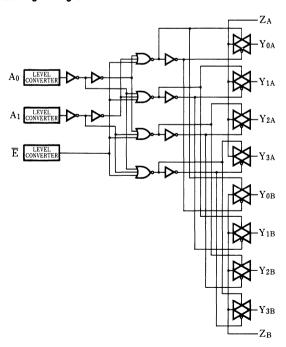
Each channel is established by controlling signals of the enable input (E). The inputs/outputs can swing between  $V_{\rm DD}$  and  $V_{\rm EE}$  ( $\leqq 15 \rm V)$  even if the amplitude of control signals is below  $V_{\rm DD}$ . It can be controlled to low impedance circuit because the impedance of the switch is very low. The MN4052B/S are equivalent to MOTOROLA MC14052B and RCA CD4052B.

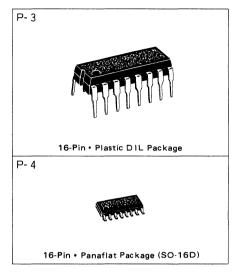
#### Truth Table

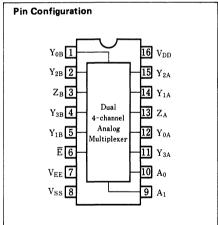
	Input	Channel ON	
Ē	A <sub>1</sub>	$A_{o}$	Channel ON
L	L	L	$Y_{oA}-Z_A; Y_{oB}-Z_B$
L	L	Н	$Y_{1A}-Z_A; Y_{1B}-Z_B$
L	Н	L	$Y_{2A}-Z_A; Y_{2B}-Z_B$
L	Н	Н	$Y_{3A}-Z_A; Y_{3B}-Z_B$
Н	×	×	All OFF

Note) X: don't care

#### Logic Diagram







#### Pin Explanation

 $Y_{0A}{\sim}\,Y_{3A}$  : Analog input/output  $Y_{0B}{\sim}\,Y_{3B}$  : Analog input/output

 $A_0, A_1$ : Address input  $\overline{E}$ : Enable input

 $Z_A$ ,  $Z_B$ : Common input/output



Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{\scriptscriptstyle  m I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	peroutput terminal)	$\mathbf{P}_{\mathrm{D}}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	<del>-65~+150</del>	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{\rm SS}{=}0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions		Ta=-40℃		Ta=25℃		Ta=85℃	
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
O : 4 P	5			$V_{ m I} \! = \! V_{ m SS}$ or $V_{ m DD}$		20		20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or			40		40		300	μA
	15					80		80	_	600	
	5		V <sub>0</sub> =0.5V or 4.5V		1.5	_	1.5		1.5		
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3		3	V
	15			Vo=1.5V or 13.5V		4		4		4	
I	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5	_	3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11		
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	V <sub>I</sub> =0 or 15V		0.3		0.3		1	μA

Item	V <sub>DD</sub> —V <sub>EE</sub> (V)	Symbol	Conditions	min.	typ.	max.	Unit	
			$V_I=5V$		200	800		
On Resistance 5	5	Ron	$V_I=2.5V$	_	550	1300	Ω	
			$V_I = 0.25V$	_	200	800		
		R <sub>on</sub>	$V_I=10V$	<del></del>	80	300		
On Resistance	10		$V_{I}=5V$	_	100	350	Ω	
			$V_{I}=0.25V$	_	80	300		
			V <sub>1</sub> =15V	_	60	200		
On Resistance	15	R <sub>on</sub>	$V_{I}=7.5V$		80	250	Ω	
			$V_{I}=0.25V$		60	200		

Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1)	5			_	10	30	
Vis→V <sub>OS</sub> (H→L)	10	t <sub>PHL</sub>	$R_L = 10k\Omega$	_	5	15	ns
VIS VOS (H-L)	15		$C_L = 50 \text{pF}$		5	15	
Propagation Delay Time (Fig. 1)	5		$\overline{E} = V_{SS}$	_	10	30	
Vis→Vos (L→H)	10	t <sub>PLH</sub>	E= vss	_	5	15	ns
VIS-VOS (L-n)	15			_	5	15	
Propagation Delay Time (Fig. 1)	5			_	150	450	
	10	tPHL	$R_L = 10k\Omega$	_	65	195	ns
$An \rightarrow V_{OS} (H \rightarrow L)$	15	j			50	150	
P (Fig. 1)	5		$ \begin{array}{l} C_{L} = 50 \text{pF} \\ \overline{E} = V_{SS} \end{array} $	_	75	225	
Propagation Delay Time (Fig. 1)	10	tplH	E=V <sub>SS</sub>	_	35	105	ns
$An \rightarrow V_{OS} (L \rightarrow H)$	15				30	90	
Output Disable Time (Fig. 1)	5				100	300	
	10	tPHZ	5 10 0	_	90	270	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15		$R_L = 10k\Omega$		90	270	
(Fig. 1)	5		$C_L = 50 pF$		95	285	
Output Disable Time (Fig. 1)	10	t <sub>PLZ</sub>	$\overline{\mathbf{E}} = \mathbf{V}_{\mathrm{DD}}$	_	90	270	ns
$E \rightarrow V_{OS}$ (L)	15			_	90	270	
(Fig. 1)	5			_	130	390	
Output Enable Time (Fig. 1)	10	tPZH	_		55	165	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15		$R_L = 10k\Omega$		45	135	
	5		$C_L = 50 pF$	_	120	360	
Output Enable Time (Fig. 1)	10	tPZL	$\overline{\mathbf{E}} = \mathbf{V}_{\mathrm{DD}}$		50	150	ns
$\overline{E} \rightarrow V_{OS}$ (L)	15			_	35	105	
	5		_		0.25		
Sine Wave Distortion (Fig. 2)	10		$R_L = 10k\Omega$ , $C_L = 15pF$		0.04		%
	15		$fis = 1 \text{ kHz}, Vis = \frac{1}{2} V_{DD (P-P)}$	_	0.04		
	5		_	_	_		
Crosstalk (Fig. 3)	10		$R_L = 1 k\Omega$	_	1	_	MHz
(Between 2 Channels)	15		$Vis = \frac{1}{2} V_{DD (P-P)}$			_	
	5		_	_			
Crosstalk (Fig. 1)	10		$R_L = 10k\Omega$ , $C_L = 15pF$		50		mV
(Address Input → Output)	15		$\overline{E}$ or $An = V_{DD}$				
	5	<u> </u>	_				
Propagation (Fig. 2) (Note 2)	10		$R_L = 1 k\Omega, C_L = 5 pF$	_	1		MHz
Frequency	15		$Vis = \frac{1}{2} V_{DD (P-P)}$	_		_	
	5				13		<b></b>
Feedthrough (Fig. 2) (Note 1)	10		$R_L = 1 k\Omega$ , $C_L = 5 pF$	_	40	_	MHz
(OFF)	15		$Vis = \frac{1}{2} V_{DD (P-P)}$	Arrahaa	70	_	
Input Capacitance	10	C <sub>I</sub>				7.5	pF
	L	1 -1		L	L		P-



Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit

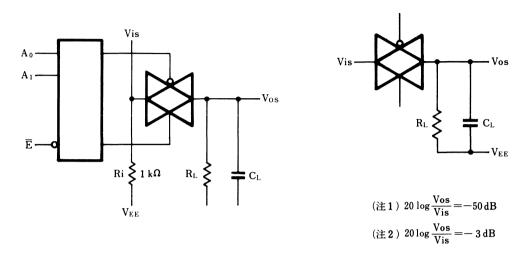
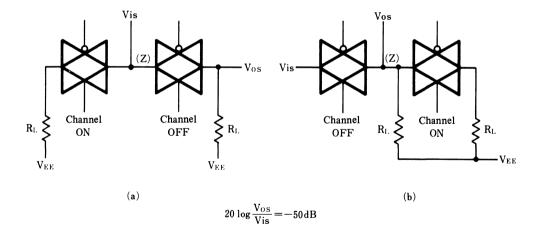


Fig. 3 Crosstalk Test Circuit



# MN4053B/MN4053BS

# Triple 2-Channel Analog Multiplexers

#### Description

The MN4053B/S are triple 2-channel analog multiplexer/demultiplexers which enable selection of digital or analog signals and their complexes.

Each channel is established by controlling signals of the enable input (E). The inputs/outputs can swing between  $V_{DD}$  and  $V_{EE}$  ( $\leq 15V$ ) even if the amplitude of control signals is below  $V_{DD}$ . It can be controlled to low impedance circuit because the impedance of the switch is very low.

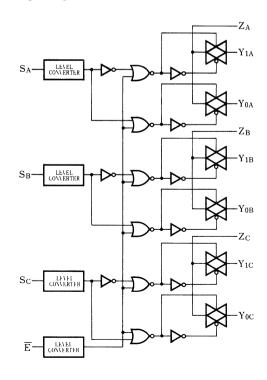
The MN4053B/S are equivalent to MOTOROLA MC14053B and RCA CD4052B.

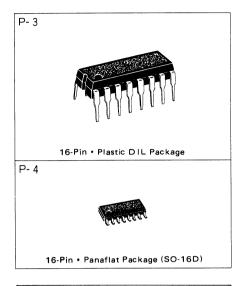
#### Truth Table

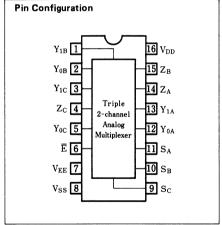
Inp	out	Channel ON			
Ē	SA	Channel ON			
L	L	Y <sub>OA</sub> -Z <sub>A</sub>			
L	Н	$Y_{1A}-Z_{A}$			
Н	×	All OFF			

Note) X: don't care

#### Logic Diagram







#### Pin Explanation

 $Y_{0A} \sim Y_{0C}$ : Analog input/output  $Y_{1A} \sim Y_{1C}$ : Analog input/output

 $\begin{array}{ccc} S_A{\sim}S_C & \text{: Select input} \\ \overline{E} & \text{: Enable input} \end{array}$ 

 $Z_A \sim Z_C$ : Common input/output

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation (per package)	Ta=-40~+60℃	n	max. 400	117
	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Itam	V <sub>DD</sub> Symbol			G1i4i		Ta=-40℃		Ta=25℃		Ta=85℃	
Item			Conditions		min.	max.	min.	max.	min.	max.	Unit
Quiescent Power	5					20		20		150	
Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
	15					80		80		600	
Input Voltage Low Level	5		$ I_0  < 1\mu A$	Vo=0.5V or 4.5V		1.5		1.5		1.5	V
	10	V <sub>IL</sub>		Vo=1V or 9V		3		3		3	
	15			Vo=1.5V or 13.5V		4		4		4	
Input Voltage High Level	5		$ I_0  < 1\mu A$	Vo=0.5V or 4.5V	3.5	_	3.5		3.5		
	10	$V_{IH}$		Vo=1V or 9V	7		7		7		V
	15			Vo=1.5V or 13.5V	11		11		11		
Input Leakage Current	15	$\pm I_I$	$V_I=0$ or 15		0.3		0.3		1	μA	

Item	V <sub>DD</sub> —V <sub>EF</sub> (V)	Symbol	Conditions	min.	typ.	max.	Unit	
On Resistance	5	R <sub>on</sub>	$V_I=5V$		200	800	Ω	
			$V_I=2.5V$	-	550	1300		
			$V_I = 0.25V$		200	800		
On Resistance	10	R <sub>on</sub>	$V_I = 10V$		80	300	350 Ω	
			$V_I = 5V$		100	350		
			$V_I=0.25V$		80	300		
On Resistance	15	R <sub>on</sub>	$V_i=15V$		60	200	Ω	
			$V_1=7.5V$		80	250		
			$V_i=0.25V$		60	200		

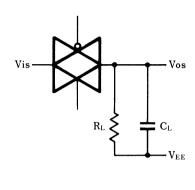
Item	$V_{DD}(V)$	Symbol	Conditions	mın.	typ.	max.	Unit
Propagation Delay Time (Fig. 1)	5				10	30	
Vis→V <sub>OS</sub> (H→L)	10 t <sub>PF</sub>	$t_{ ext{PHL}}$	$R_L = 10k\Omega$	_	5	15	ns
VIS-VOS (II-L)	15		$C_L = 50 \text{pF}$	_	5	15	ns
Propagation Delay Time (Fig. 1)	5		$\overline{E} = V_{DD}$	_	10	30	n
Propagation Delay Time $V_{\text{is}} \rightarrow V_{\text{OS}}$ (L $\rightarrow$ H)	10	t <sub>PLH</sub>	E=VDD	_	5	15	ns
VIS VOS (L H)	15			_	5	15	n
P (Fig 1)	5			_	200	600	n
Propagation Delay Time (Fig. 1) $Sn \rightarrow V_{OS}$ (H $\rightarrow$ L)	10	tpHL	B 101.0		85	255	ns
Sn→Vos (H→L)	15		$R_L = 10k\Omega$	_	65	195	n
(Fig. 1)	5		$C_L = 50 pF$		275	725	%
Propagation Delay Time (Fig. 1)	10	tPLH	$\bar{\mathbf{E}} = \mathbf{V}_{SS}$	_	100	300	ns
$Sn \rightarrow V_{OS} (L \rightarrow H)$	15			*********	65	195	
Output Disable Time (Fig. 1)	5			_	200	600	
	10	tPHZ	D 1010		115	345	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15		$R_L = 10k\Omega$	_	110	330	
Company (Fig. 1)	5		$C_L = 50 pF$	_	200	600	
Output Disable Time (Fig. 1)	10	tPLZ	$\overline{E} = V_{DD}$	_	120	360	ns
$\overline{E} \rightarrow V_{OS}$ (L)	15				110	330	
(Fig. 1)	5				260	780	
Output Enable Time (Fig. 1)	10	tPZH	_		95	285	ns
$\overline{E} \rightarrow V_{OS}$ (H)	15		$R_L = 10k\Omega$	******	65	195	
(Fig. 1)	5		$C_L = 50pF$ $\overline{E} = V_{DD}$		280	840	
Output Enable Time (Fig. 1)	10	tPZL			105	315	ns
$\overline{E} \rightarrow V_{0S}$ (L)	15	-1 2.5			70	210	
	5				0.25	_	
Sine Wave Distortion (Fig. 2)	10		$ \begin{vmatrix} R_L = 10k\Omega, & C_L = 15pF \\ fis = 1 & kHz \end{vmatrix} $		0.04	_	%
	15				0.04		
	5		_				
Crosstalk (Fig. 3)	10		$R_L = 1 k\Omega$		1	_	MHz
(Between 2 Channels)	15		$Vis = \frac{1}{2} V_{DD (P-P)}$		_		
	5				_		
Crosstalk (Fig. 1)	10		$ \begin{array}{c} R_L \! = \! 10k\Omega,  C_L \! = \! 15pF \\ \overline{E}n \text{ or } Sn \! = \! V_{DD} \end{array} $		50		mV
(Address Input → Output)	15			_	_		
	5		, , , , , , , , , , , , , , , , , , ,				
Feedthrough (Fig. 2) (Note 1)	10		_		1		MHz
(OFF)	15		$R_L = 1 k\Omega$		_	_	
	5		$\begin{split} &C_L = 5 \ pF \\ &Vis = \frac{1}{2} V_{DD \ (P-P)} \end{split}$		13	_	
Propagation (Fig. 2) (Note 2)	10				40	_	MHz
Frequency	15			_	70	_	
Input Capacitance	1	Cı		_	_	7.5	pF



Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

 $V_{\rm EE}$ 

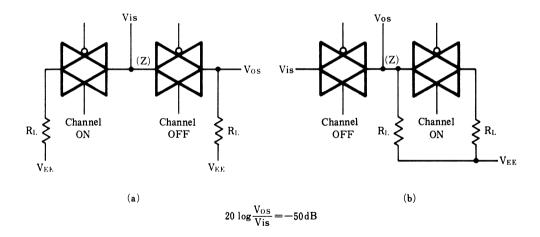
Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit



(注1)
$$20 \log \frac{Vos}{Vis} = -50 dB$$

(注 
$$2$$
)  $20 \log \frac{\mathrm{Vos}}{\mathrm{Vis}} = -3 \,\mathrm{dB}$ 

Fig. 3 Crosstalk Test Circuit



# MN4066B/MN4066BS

## Quad Analog Switches

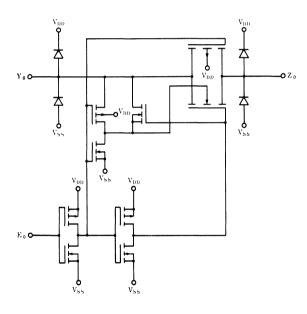
#### Description

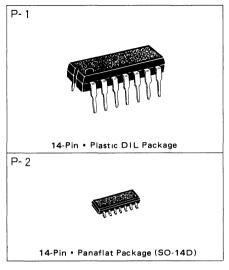
The MN4066B/S have 4 independent analog switches. A High on the enable input establishes a low impedance state (ON stage) between input and output of the switch. A Low establishes a high impedance (OFF stage).

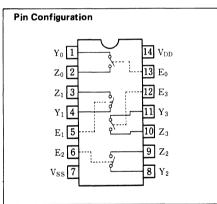
MN4066B is pin-compatible to MN4016B. But MN4066B has low  $R_{\mbox{ON}}$  and better transfer characteristics. So applications are for analog/digital switching and chopper modulation and demodulation.

The MN4066B/S are equivalent to MOTOROLA MC14066B and RCA CD4066B.

#### Schematic Diagram (1/4)







#### Pin Explanation

 $E_0 \sim E_3$ : Enable input

 $Y_0 \sim Y_3$ : Analog input/output  $Z_0 \sim Z_3$ : Analog input/output



### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	n	max. 400	117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (peroutput terminal)		$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS} {=} 0V)$

14	$V_{DD}$	Sym-		1 4:4:	Ta=-	- <b>40</b> ℃	Ta=25℃		Ta=	<b>85</b> ℃	Unit
Item	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Onit
O :	5					1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	=V <sub>SS</sub> or V <sub>DD</sub>		2		2		15	μA
	15					4		4		30	
	5			V <sub>0</sub> =0.5V or 4.5V		1.5	-	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	_	3		3		3	V
	15			Vo=1.5V or 13.5V		4		4		4	
T	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11	_	
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	V.		0.3		0.3		1	μA

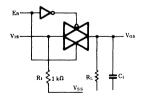
## $\blacksquare$ DC Characteristics (Ta=25°C, V<sub>SS</sub>=0V)

Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit
			$V_{SS}=0V, V_{I}=5V$	-	150	450	
	5	R <sub>on</sub>	$V_{SS}=0V$ , $V_{I}=2.5V$	_	380	1140	Ω
			$V_{SS}=0V, V_{I}=0.25V$		150	450	
	10		$V_{SS}=0V$ , $V_I=10V$		80	250	
		Ron	$V_{SS}=0V, V_{I}=5V$	_	100	300	Ω
			$V_{SS}=0V, V_{I}=0.25V$		100	300	
	15	R <sub>on</sub>	$V_{SS}=0V$ , $V_I=15V$		60	180	
On Resistance			$V_{SS}=0V, V_{I}=7.5V$		70	210	Ω
			$V_{SS} = 0V, V_{I} = 0.25V$		60	180	
		R <sub>on</sub>	$V_{SS}=-5V$ , $V_I=5V$	<del></del>	100	300	
	5		$V_{SS} = -5V, V_{I} = \pm 0.25V$		100	300	Ω
			$V_{SS}=-5V$ , $V_I=-5V$	Militare	100	300	
			$V_{SS} = -7.5V, V_{I} = 7.5V$		70	210	
	7.5	Ron	$V_{SS} = -7.5V, V_{I} = \pm 0.25V$		70	210	Ω
			$V_{SS} = -7.5V, V_{I} = -7.5V$		70	210	
	10		$V_{I}=10V, V_{0}=0V$		30	125	nA
Input Output of Leakage Current	10	,	$V_I$ =0V, $V_O$ =10V		30	125	IIA
	15	I <sub>OFF</sub>	$V_I$ =15V, $V_O$ =0V		60	250	nA
	15		$V_I$ =0V, $V_0$ =15V		60	250	IIA

## Switching Characteristics ( $T_a=25$ °C, $V_{SS}=0V$ )

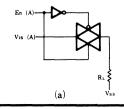
Item	$V_{DD}(V)$	Symbol	Conditions	min.	typ.	max.	Unit
- (Fig. 1)	5				10	30	
Propagation Delay Time (Fig. 1) Vis→V <sub>OS</sub>	10	tPHL	$R_1 = 10k\Omega$	_	5	15	ns
V 15 - V 05	15		$C_L = 50 pF$		5	15	
Propagation Delay Time (Fig. 1)	5		$E_{\rm n} = V_{\rm DD}$	_	10	30	
Vis→Vos	10	tplH	En— VDD		5	15	ns
V 15 V V U S	15			_	5	15	
n n (Fig. 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	80	240	
Propagation Delay Time <sup>(Fig. 1)</sup> En→Vos	10	tPHZ	$Vis = V_{DD}  R_L \rightarrow V_{SS}$		65	195	ns
Lii · Vos	15		VIS VDD, ILL VVSS		60	180	
- (Fig. 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	80	240	
Propagation Delay Time (Fig. 1) En \(\to V_{OS}\)	10	t <sub>PLZ</sub>	$V_{is} = V_{SS}, R_{L} \rightarrow V_{DD}$	_	70	210	ns
En- vos	15		VIS - VSS, IL - VBB	_	70	210	
Properties Del Tri (Fig. 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	40	120	
Propagation Delay Time (Fig. 1) En→V <sub>0S</sub>	10	t <sub>PZH</sub>	$Vis = V_{DD}, R_L \rightarrow V_{SS}$		20	60	ns
	15		VIS - VDD, KL - VSS	_	15	45	
Propagation Delay Time (Fig. 1)	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	45	135	
En→Vos	10	tpzL	$V_{is} = V_{SS}  R_{L} \rightarrow V_{DD}$		20	60	ns
En-+ vos	15		VIS – VSS, ILL – VDD		15	45	
	5		$R_L = 10k\Omega$ , $C_L = 50pF$	_	_		
Sine Wave Distortion (Fig. 2)	10		$E_n = V_{DD}$ , $f = 1 \text{ kHz}$		0.1		%
	15		$Vis = \frac{1}{2} V_{DD(P \cdot P)}$		0.1		
(Fig. 3)	5		$R_L = 1 k\Omega$	_			
Crosstalk (Fig. 3) (Between 2 Channels)	10		$Vis = \frac{1}{2} V_{DD (P-P)}$	_	1	_	MHz
(Between 2 Chaineis)	15		VIS — 2 VDD (P-P)	_	_		
Crosstalk (Fig. 1)	5		$R_L = 1 k\Omega$ , $C_L = 15 pF$	_	_		
	10		$E_{\rm n} = V_{\rm DD}$	_	80	_	mV
Æn→Vss	15		Eu = ADD	_	_		
(Fig. 2)(No+a)	5		$R_L = 1 k\Omega$ , $C_L = 50 pF$		_		
Feedthrough (Fig. 2) (Note) (OFF)	10	1	/	_	700		kHz
(011)	15		$E_{n} = V_{SS}$ , $V_{is} = \frac{1}{2} V_{DD(P \cdot P)}$			_	
Input Capacitance		Cı		_		7.5	pF

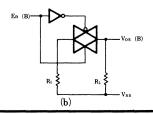
Fig. 1 Propagation Delay Time, Crosstalk Test Circuit Fig. 2 Sine Wave Distortion, Feedthrough Test Circuit



 $V_{1s} = V_{0s}$   $V_{1s} = V_{0s}$   $V_{0s} = V_{0s}$ 

Fig. 3 Crosstalk Test Circuit





 $20 \log \frac{\text{Vos } (B)}{\text{Vis } (A)} = -50 \text{dB}$ 

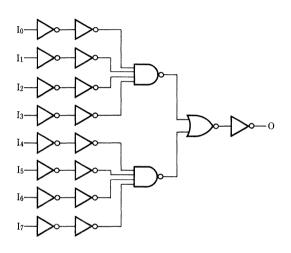
## MN4068B/MN4068BS

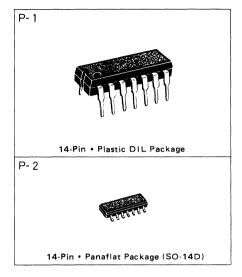
## 8-Input NAND Gates

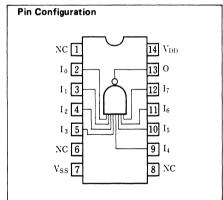
#### Description

The MN4068B/S are positive 8-input NAND gates. The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time.

#### Logic Diagram







Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	Λ,
Peak Input · Output	t Current	±Ιι	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	11.
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

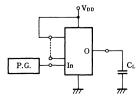
## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	77.14
ntem	(V)	bol		min.	max.	min.	max.	min.	max.	Unit	
Oni-	5					1		1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS} \text{ or } V_{DD}$		_	2		2	_	15	μA
	15			_	4		4	_	30		
	5		V-V	37	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	$v_{ m DD}$		0.05	-	0.05	_	0.05	V
Bow Bover	15		$ I_0  < 1\mu A$		_	0.05	_	0.05	_	0.05	
_	5		$V_I = V_{SSOr}$	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>		V DD	9.95		9.95		9.95	_	v
	15		$ I_0  < 1\mu A$		14.95		14.95		14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	-	3	-	3	v
2011 2011	15			V <sub>0</sub> =1.5V or 13.5V		4		4	_	4	
	5			Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7		v
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11		11	_	
	5		$V_0 = 0.4V$ ,	$V_I$ =0 or 5V	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9	-	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6		3		2.4	_	
	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I$ =0 or 10V	1.3	_	1.1	_	0.9	-	mA
15			$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4	_	
Output Current High Level	5	—I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	V	-	0.3		0.3	_	1	μA

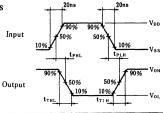
### **Switching Characteristics** $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
Output Fall Time	5		_	60	180	
	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
	5			95	285	
Propagation Delay Time	10	t <sub>PHL</sub>	_	40	120	ns
$I-O (H\rightarrow L)$	15		-	30	90	
D D 1	5		_	80	240	
Propagation Delay Time I—O (L→H)	10	tPLH	_	35	105	ns
	15		_	30	90	
Input Capacitance		Cı	_	_	7.5	pF

#### 1. Switching Time Test Circuit



#### 2. Waveforms





## MN4069UB/MN4069UBS

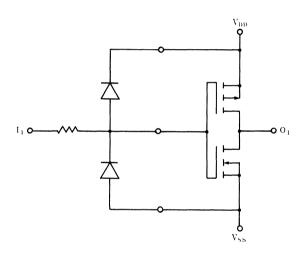
### Hex Inverters

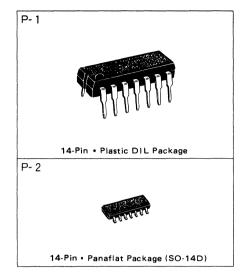
#### Description

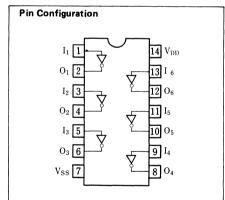
The MN4069UB/S have hex inverters without buffers. The MN4069UB has a single-stage gate and therefore a short transient time

They are equivalent to MOTOROLA MC14069UB and RCA CD4069UB.

#### Schematic Diagram (1/6) & Input Protection Circuit







#### Maximum Ratings $(Ta=25^{\circ}C)$

Item	1	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{\rm o}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	m vv
Power Dissipation (pe	er output terminal)	$P_{D}$	max. 100	mW
Operating Ambient T	Temperature	Topr	-40~+85	°C
Storage Temperature	;	Tstg	-65~+150	°C

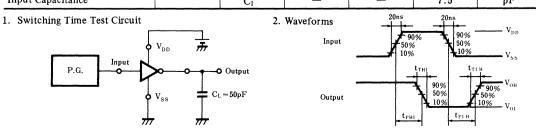
<sup>\*</sup> VDD + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	***
ntem	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Unit
	5				_	1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2	_	2	_	15	μA
	15					4		4		30	
	5		V — V	V		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_i = V_{SS}$ or	$V_{ m DD}$		0.05		0.05	_	0.05	v
Low Level	15		$ I_{\rm o}  < 1\mu A$			0.05		0.05		0.05	
	5		37 — 37	V	4.95	_	4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SSOI}$	V DD	9.95		9.95		9.95		v
mg. Lover	15		$ I_{\rm o}  < 1\mu A$		14.95	_	14.95		14.95		
	5			Vo=0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3	<u> </u>	3		3	V
Low Level	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5	_	3.5		
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		v
	15			Vo=1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44	_	0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I$ =0 or 10 $V$	1.3		1.1		0.9	_	mA
2011 20101	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6 V$	V <sub>I</sub> =0 or 5V	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	V <sub>I</sub> =0 or 10V	1.3		1.1		0.9		mA
Tigit Lovel	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	SV .		0.3		0.3	_	1	μA

## Switching Characteristics ( $Ta = 25^{\circ}C$ , $V_{SS} = 0V$ , $C_L = 50pF$ )

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit											
	5			60	180												
Output Rise Time	10	$t_{\mathrm{TLH}}$	_	30	90	ns											
	15		_	20	60												
Output Fall Time	5		_	60	180												
	10	t <sub>THL</sub>	_	30	90	ns											
	15		_	20	60												
	5		_	40	120												
Propagation Delay Time	10	t <sub>PLH</sub>	_	20	60	ns											
	15		_	15	45												
	5		_	45	135												
Propagation Delay Time	10	t <sub>PHL</sub>	t <sub>PHL</sub>	$\mathbf{t}_{\mathtt{PHL}}$	$\mathbf{t}_{\mathtt{PHL}}$	t <sub>PHL</sub>	$t_{ ext{PHL}}$	t <sub>PHL</sub>	t <sub>PHL</sub>	$t_{ ext{PHL}}$	$t_{ ext{PHL}}$	t <sub>PHL</sub>	$\mathbf{t}_{\mathtt{PHL}}$	_	20	60	ns
	15		_	15	45												
Input Capacitance		Cı	_	_	7.5	pF											





## MN4071B/MN4071BS

## Quad 2-Input OR Gates

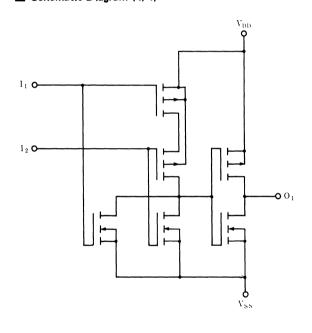
#### Description

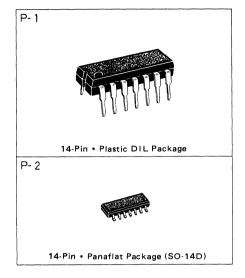
The MN4071B/S are positive 2-input OR gates and have 4 circuits in a package.

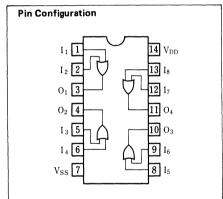
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4071B/S are equivalent to MOTOROLA MC14071B and RCA CD4071B.

#### Schematic Diagram (1/4)







Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	$\pm I_{\mathfrak{l}}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	. 117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	°C

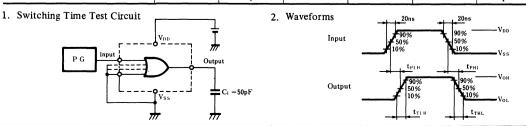
<sup>\*</sup> VDD + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	$V_{DD}$	Sym-			Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Oiiit
O : P	5				_	1	-	1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		2	_	2		15	μA
	15					4	_	4		30	
	5		$V_I = V_{SS}$ or	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	V <sub>DD</sub>	-	0.05		0.05		0.05	v
20.1.20.01	15		$ 1_0  < 1\mu A$		-	0.05	_	0.05	_	0.05	
0	5		$V_I = V_{SS}$ or	37	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$ I_{\rm O}  < 1\mu A$	V DD	9.95	_	9.95	_	9.95		v
	15		10  < 1µA		14.95		14.95		14.95	_	
	5			Vo=0.5V or 4.5V	-	1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O} \!<\!1\mu A$	Vo=1V or 9V	_	3	_	3	_	3	v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4	_	4	_	4	
	5			Vo=0.5V or 4.5V	3.5		3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7		7		v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11		11	-	
	5		$V_0=0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36	_	
Output Current Low Lèvel	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10V$	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15V	3.6	_	3	_	2.4	_	
	5		$V_0 = 4.6 V$ ,	$V_I = 0$ or $5V$	0.52	_	0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3	_	1.1	_	0.9		mA
	$V_0=13.5V, V_I=0 \text{ or } 15V$		3.6	_	3	_	2.4				
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	V		0.3	_	0.3		1	μA

## ■ Switching Characteristics $(Ta=25^{\circ}C, V_{SS}=0V, C_{L}=50pF)$

Item	$V_{\mathrm{DD}}\left( V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
	5		_	55	165	
Propagation Delay Time	10	$\mathbf{t}_{\mathtt{PLH}}$		25	75	ns
	15		_	20	60	
	5			45	135	
Propagation Delay Time	10	$t_{ ext{PHL}}$	_	20	60	ns
	15			15	45	
Input Capacitance		Cı	_	_	7.5	pF



## MN4072B / MN4072BS

Dual 4-Input OR Gates

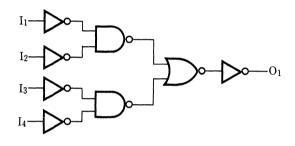
#### Description

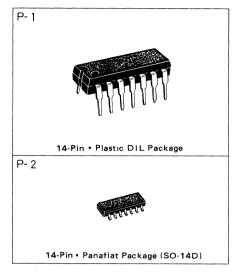
The MN4072B/S are positive 4-input OR gates and have 2 circuits in a package.

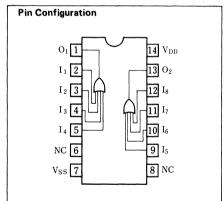
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4072B/S are equivalent to MOTOROLA MC14072B and RCA CD4072B.

#### Logic Diagram (1/2)







Ite	em	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	337
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatu	re	Tstg	-65~+150	°C

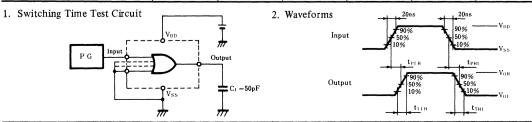
<sup>\*</sup> VDD + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

14	$V_{ m DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
	5				_	1		1	_	7.5	
Quiescent Power Supply Current	10	$I_{D\bar{D}}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2		2	_	15	μA
	15				_	4		4		30	
	5		V - V	V	_	0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	. 55	$V_{\rm I} = V_{\rm SS}  \text{or}  V_{\rm DD}$		0.05		0.05		0.05	V
	15		$ I_{\rm o}  < 1\mu A$			0.05	_	0.05		0.05	
	5		V – V	17	4.95		4.95		4.95		
Output Voltage High Level	10	Voh	$ V_I=V_{SS}$ or $ I_O <1\mu A$	V DD	9.95	-	9.95		9.95		V
	15		$ 1_0  < 1\mu A$		14.95		14.95		14.95		
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3		3	V
	15			Vo=1.5V or 13.5V		4		4	-	4	
Y X7 14	5			Vo=0.5V or 4.5V	3.5	-	3.5		3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			Vo=1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36		
Output Current Low Level	10	IoL	$V_0=0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6	-	3		2.4	_	
	5		$V_0 = 4.6 V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I = 0$ or $5V$	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0$ or 15	SV.	_	0.3	_	0.3	_	1	μA

## ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	$t_{TLH}$	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5		_	75	225	
Propagation Delay Time	10	$\mathbf{t}_{\mathtt{PLH}}$		35	105	ns
	15		_	25	75	
	5		_	80	240	
Propagation Delay Time	10	t <sub>PHL</sub>	_	35	105	ns
	15			25	75	
Input Capacitance		Cı	_		7.5	pF





## MN4073B/MN4073BS

## Triple 3-Input AND Gates

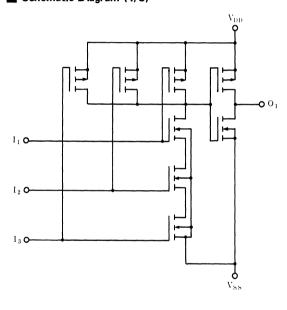
#### Description

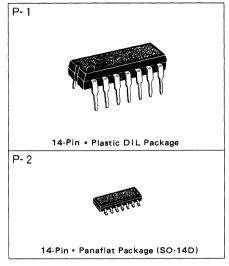
The MN4073B/S are positive 3-input AND gates and have 3 circuits in a package.

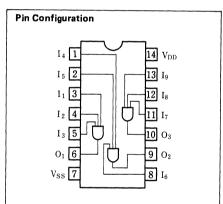
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4073B/S are equivalent to MOTOROLA MN14073B and RCA CD4073B.

### Schematic Diagram (1/3)







Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	-0.5~V <sub>DD</sub> +0.5*	V
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	$^{\circ}$
Storage Temperatur	re	Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

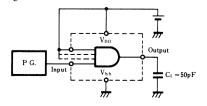
## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

*****	$V_{\mathrm{DD}}$	Sym-		1	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	T I = : 4
Item	(V)	bol	C	onditions	min.	max.	min.	max.	min.	max.	Unit
0	5				_	1	_	1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_l = V_{SS or}$	$V_{DD}$		2	_	2		15	μA
	15				_	4	_	4	_	30	
	5		V-V	<b>V</b>	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	$v_{ m DD}$	_	0.05		0.05	_	0.05	V
2011 20101	15		$ 1_0  < 1\mu A$			0.05	_	0.05		0.05	
	5		V V	17	4.95	_	4.95		4.95		
Output Voltage High Level	10	VoH	$V_I = V_{SS}$ or	V DD	9.95		9.95	_	9.95		V
	15		$ I_{\rm O}  < 1\mu A$		14.95		14.95	_	14.95		
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V
20 11 20 101	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4	_	4		4	
	5			Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11	_	11	_	
	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52	_	0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9		mA
20 11 20 101	15		$V_0 = 1.5V$ ,	$V_I = 0 \text{ or } 15 \text{V}$	3.6		3	_	2.4	_	
_	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44	-	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
	15		Vo=13.5V	, $V_I$ =0 or 15 $V$	3.6	_	3	_	2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	±Ιι	V <sub>I</sub> =0 or 15	SV		0.3		0.3		1	μA

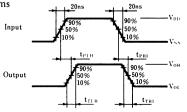
#### Switching Characteristics ( $Ta = 25^{\circ}C$ , $V_{SS} = 0V$ , $C_L = 50pF$ )

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit	
	5		_	60	180		
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns	
	15			20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns	
	15		_	20	60		
	5			55	165		
Propagation Delay Time	10	t <sub>PIH</sub>		25	75	ns	
	15			20	60		
	5			45	135		
Propagation Delay Time	10	t <sub>PHL</sub>	_	20	60	ns	
	15			15	45		
Input Capacitance		Cı			7.5	pF	

1. Switching Time Test Circuit



2. Waveforms Input



## MN4075B/MN4075BS

## Triple 3-Input OR Gates

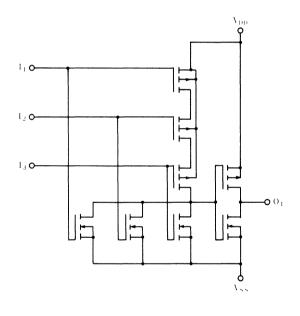
#### Description

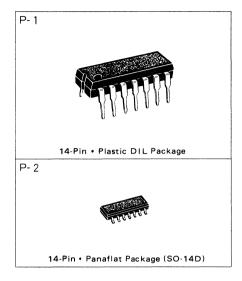
The MN4075B/S are positive 3-input OR gates and have 3 circuits in a package.

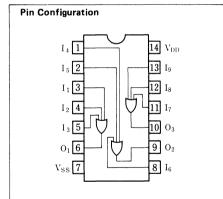
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4075B/S are equivalent to MOTOROLA MC14075B and RCA CD4075B.

#### Schematic Diagram (1/3)







Ite	m	Symbol	Ratings	Unit
Supply Voltage	Supply Voltage		-0.5~+18	V
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	W
(per package)	Ta=+60~+85℃	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	$-65 \sim +150$	$^{\circ}$

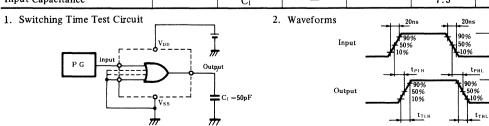
<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	,	Conditions	min.	max.	min.	max.	min.	max.	Unit
O :	5					1	_	1		7.5	
Quiescent Power Supply Current	10	I <sub>DD</sub>	$V_{I} = V_{SS}$ or	$V_{DD}$	_	2		2		15	μA
	15				_	4		4		30	
	5		$V_I = V_{SS}$ or	V	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1 \mu A$	VDD		0.05	_	0.05	_	0.05	V
20.1. 20.101	15		1 <sub>0</sub>   < 1µA			0.05		0.05		0.05	
	5		$V_i = V_{ssor}$	V	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	V DD	9.95	_	9.95		9.95	!	v
	15		10  < 1 µA		14.95	_	14.95	_	14.95	_	
	5			Vo=0.5V or 4.5V	_	1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4	_	4	
Y X7 14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7	-	7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I$ =0 or 10V	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15V	3.6	_	3		2.4		
	5		$V_0 = 4.6 V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6		3		2.4	_	
Output Current High Level	5	—I <sub>он</sub>	$V_0 = 2.5 V$ ,	$V_I = 0 \text{ or } 5V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	SV .	_	0.3		0.3		1	μA

## 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		-	20	60	
	5			65	195	
Propagation Delay Time	10	t <sub>PLH</sub>	_	30	90	ns
	15		_	25	75	
	5		<del>-</del>	65	195	
Propagation Delay Time	10	t <sub>PHL</sub>		30	90	ns
	15		_	20	60	
Input Capacitance		Cı	_	_	7.5	pF





## MN4076B/MN4076BS

## 4-Bit D-Type Registers

#### Description

The MN4076B/S are 4-bits registers composed of quad D-type flip-flops with tristate outputs and controlled by the common clock and reset inputs.

All inputs  $(D_0 \sim D_3)$  are stored in four flip-flops on the positive going edge of the clock, when the data enable inputs  $(\overline{EO}_0, \overline{ED}_1)$  are Low.

In other combinations of the data enable inputs, 4 flip-flops hold the previous stage even after the going edge of the clock.

When output enable inputs  $(\overline{EO}_0, \overline{EO}_1)$  are Low, each flip-flop's outputs are from  $O_0 \sim O_3$ .

In other combinations of the output enable inputs, all outputs are High impedance.

A High on the reset input makes outputs Low asynchronously.

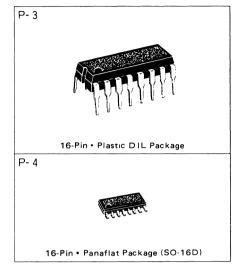
The MN4076B/S are equivalent to MOTOROLA MN14076B and RCA CD4076B.

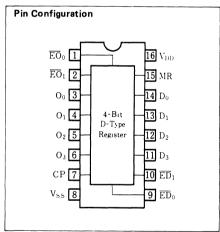
#### Truth Table

			Input				Output
MR	CP	$\overline{\mathrm{ED_0}}$	$\overline{\mathrm{ED_{1}}}$	$D_{o}$	EO <sub>0</sub>	$\overline{\mathrm{EO}}_{\scriptscriptstyle 1}$	O <sub>0n+1</sub>
	×	×	×	×	Н	×	Z
×	×	×	×	×	×	Н	Z
Н	×	×	×	×	L	L	L
L		Н	×	×	L	L	no change
L		×	Н	×	L	L	no change
L		L	L	Н	L	L	Н
L		L	L	L	L	L	L
L	_	×	×	×	L	L	no change
L	×	×	×	×	L	L	no change

Note) X: don't care

Z : high impedance





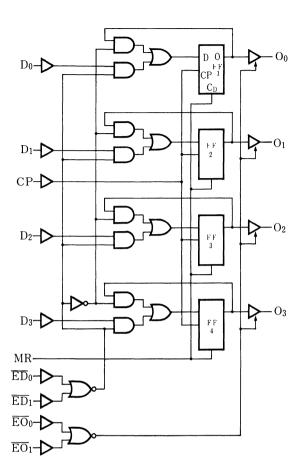
#### Pin Explanation

 $\begin{array}{ll} D_0 {\sim} D_3 & \vdots & \text{Data input (4 Bits)} \\ \overline{ED_0}, \overline{ED_1} & \vdots & \text{Data enable input} \\ \overline{EO_0}, \overline{EO_1} & \vdots & \text{Output enable input} \end{array}$ 

CP : Clock input MR : Reset input

 $O_0 \sim O_3$ : Data output (4 Bits)

### Logic Diagram



Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V	
Input Voltage		VI	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_1$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D.	max. 400	117	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	$^{\circ}$	
Storage Temperature		Tstg	-65~+150	$^{\circ}$	

 $<sup>*</sup>V_{DD} + 0.5V$  should be under 18V



## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

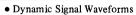
Item	$V_{DD}$	Sym-	_	Conditions	Ta=-	- <b>40℃</b>	Ta=	25℃	Ta=	85℃	T 1 :-
Item	(V)	bol		onditions	min.	max.	min.	max.	min.	max.	Unit
Quiescent Power	5					20		20	_	150	
Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$		40		40		300	$\mu$ A
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	VoL	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	$\mathbf{v}_{\mathrm{DD}}$		0.05	_	0.05	-	0.05	V
	15		$ 1_0  < 1\mu A$			0.05		0.05	_	0.05	
	5		V-V	17	4.95	_	4.95		4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	$V_{ m DD}$	9.95		9.95		9.95		V
	15		$ I_0  < 1\mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1 \mu A$	Vo=1V or 9V		3		3	-	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4	_	4		4	
T	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11	-	11		
_	5		$V_0 = 0.4 V$ ,	$V_I = 0$ or $5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5V$ ,	$V_I = 0$ or $10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \text{V}$	3.6		3		2.4	_	
0 0	5		$V_0 = 4.6V$	$V_I$ =0 or 5 $V$	0.52	_	0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0$ or $10 \text{V}$	1.3		1.1	-	0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3	********	2.4		
Output Current High Level	5	$-I_{OH}$	$V_0=2.5V$ ,	$V_I$ =0 or 5 $V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_i = 0 \text{ or } 15$	SV	_	0.3		0.3		1	μA
3-State Leakage Current High Level	15	$I_{OZH}$	$V_{O}=V_{DD}$			1.6	_	1.6		12	μA
Output'Pin Leakage Current Low Level	15	$-I_{\rm ozL}$	$V_0 = V_{SS}$			1.6	_	1.6	_	12	μΛ

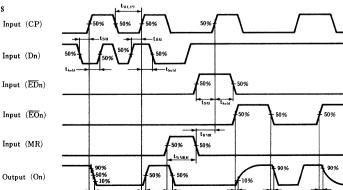
## 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5		-	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	150	450	
CP→On (H→L)	10	$t_{ m PHL}$		60	180	ns
CP→On (H→L)	15			45	135	
Dunantian Dalay Time	5		_	160	480	
Propagation Delay Time CP→On (L→H)	10	t <sub>PLH</sub>	_	65	195	ns
CP→On (L→H)	15			45	135	
Propagation Delay Time	5		_	95	285	
opagation Delay Time	10	t <sub>PHL</sub>	_	40	120	ns
$MR \rightarrow On (H \rightarrow L)$	15		_	30	90	

## ■ Switching Characteristics $(Ta=25^{\circ}C, V_{SS}=0V, C_{L}=50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Item	5	39111001		50	150	Oin
High Level Output Disable Time	5 10			35	105	nc
<del>EO</del> n→On (H)	10 15	t <sub>PHZ</sub>	_	30	90	ns
Low Level Output Disable Time	5		_	45	135	
<del>EO</del> n→On (L)	10	t <sub>PLZ</sub>	_	30	90	ns
	15			30	90	
High Level Output Enable Time	5			65	195	
EOn→On (H)	10	t <sub>PZH</sub>	_	30	90	ns
	15			20	60	
Low Level Output Enable Time	5			60	180	
EOn→On (L)	10	t <sub>PZL</sub>	_	25	75	ns
EOII-OII (E)	15		_	20	60	
Sat Time-	5		_	-15	10	
Set-up Time	10	tsu	_	-10	0	ns
Dn→CP	15		_	- 5	0	
g	5		_	-50	0	
Set-up Time	10	tsu		-20	0	ns
EDn→CP	15			-15	0	
	5		-	30	55	
Hold Time	10	thold		10	20	ns
Dn→CP	15	, and the		10	15	
	5			-25	25	
Hold Time	10	thold		-10	10	ns
EDn→CP	15	lioid		<b>– 5</b>	5	
	5			60	180	
Low Level Minimum Clock	10	twcpl		20	60	ns
Pulse Width	15	WCPL	_	15	45	5
	5			25	75	
High Level Minimum MR	10		_	15	45	ns
Pulse Width		t <sub>wmrh</sub>		10		118
	15				30	
	5		4	8		
Maximum Clock Frequency	10	fmax.	11	22	_	MHz
	15		16	32		
Input Capacitance		$C_{I}$	_	_	7.5	pF







## MN4078B/MN4078BS

## 8-Input NOR Gates

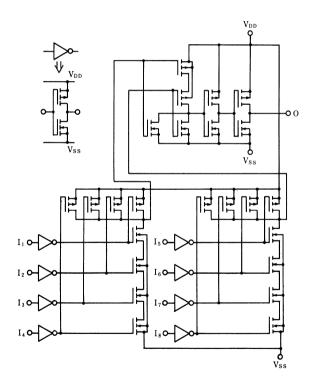
### Description

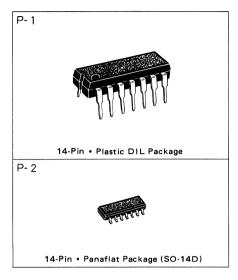
The MN4078B/S are positive 8-input NOR gates.

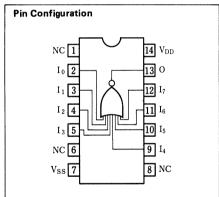
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4078B/S are equivalent to MOTOROLA MC14078B and RCA CD4078B.

#### Schematic Diagram







## $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Iter	n	Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{\rm o}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (p	er output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	$-65 \sim +150$	$^{\circ}$

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	**
	( <b>V</b> )	bol	`	Conditions	min.	max.	min.	max.	min.	max.	Unit
Ouiescent Power	5				_	1	_	1	_	7.5	
Supply Current	10	$I_{DD}$	$V_l = V_{SS}$ or	$V_{\text{DD}}$		2		2	_	15	μA
	15					4		4	_	30	
	5		$V_i = V_{SS}$ or	17	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1\mu$ A	$v_{ m DD}$		0.05	_	0.05		0.05	v
	15		$ 1_0  < 1\mu A$		_	0.05	_	0.05		0.05	
	5		V <sub>I</sub> =V <sub>SS</sub> or	17	4.95	_	4.95		4.95		
Output Voltage High Level	10	Von	$ V_I - V_{SS}$ or $ I_O  < 1 \mu A$	V DD	9.95		9.95	_	9.95	_	V
	15		$ 10  < 1\mu A$		14.95		14.95	_	14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	_	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4		4	_	4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11	_	
_	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52	_	0.44	_	0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9	_	mA
2011 20101	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6 V$	$V_I = 0$ or $5V$	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I$ =0 or 10V	1.3		1.1	_	0.9		mA
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_I$ =0 or 15	SV .	_	0.3	_	0.3	_	1	μA

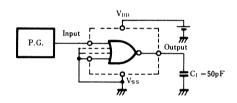


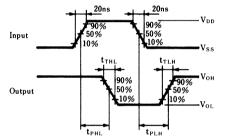
Switching Characteristics  $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$ 

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	tTLH		30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5		_	80	240	
Propagation Delay Time	10	t <sub>PLH</sub>		35	105	ns
	15			25	75	
	5			80	240	
Propagation Delay Time	10	t <sub>PHL</sub>		35	105	ns
	15		_	25	75	
Input Capacitance		Cı			7.5	pF

### 1. Switching Time Test Circuit

#### 2. Waveforms





## MN4081B / MN4081BS

## Quad 2-Input AND Gates

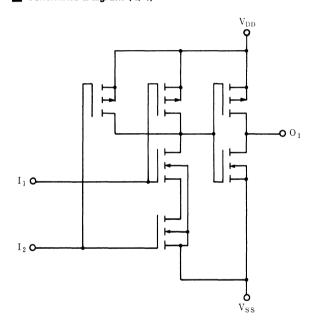
#### Description

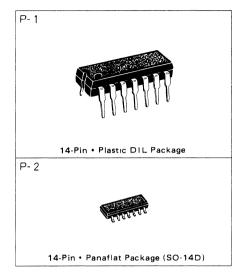
The MN4081B/S are positive 2-input AND gates and have 4 circuits in a package.

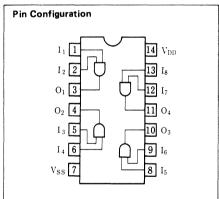
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4081B/S are equivalent to MOTOROLA MC14081B and RCA CD4081B.

#### ■ Schematic Diagram (1/4)







Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		V <sub>1</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	± I1	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D.	max. 400	117
(per package)	Ta=+60~+85°C	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_{\mathrm{D}}$	max. 100•	mW
Operating Ambient Temperature		Topr	<b>−40~+85</b>	°C
Storage Temperatur	e	Tstg	$-65 \sim +150$	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V



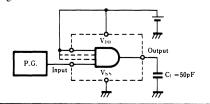
## ■ DC Characteristics (V<sub>SS</sub>=0V)

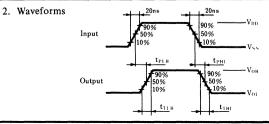
Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25℃</b>	Ta=	85℃	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
O :	5					1	_	1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2	_	2	<b> </b>	15	μA
	15				_	4	_	4	-	30	
	5		37 — 37		_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	$V_{ m DD}$		0.05	_	0.05	_	0.05	V
Low Level	15	İ	$ I_0  < 1\mu A$		_	0.05	_	0.05	—	0.05	1
	5		37 — 37	V	4.95		4.95		4.95	_	
Output Voltage High Level	10	Voh	$V_I = V_{SS}$ or	V DD	9.95		9.95	_	9.95		V
	15		$ I_0  < 1\mu A$		14.95		14.95		14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	V <sub>IL</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	_	3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4	_	4	
	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5	_	3.5		
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11	_	11		
	5		$V_0 = 0.4V$	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I$ =0 or 10V	1.3	_	1.1	_	0.9		mA
20 11 20 101	15		$V_0 = 1.5 V$	$V_l$ =0 or 15V	3.6	_	3	_	2.4	_	
	5		$V_0 = 4.6V$	V <sub>I</sub> =0 or 5V	0.52	_	0.44	_	0.36		
Output Current High Level	10	—Іон	$V_0 = 9.5V$	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
	15		Vo=13.5V	$V_{I}=0 \text{ or } 15V$	3.6	_	3	_	2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	5V	_	0.3		0.3	_	1	μA

#### Switching Characteristics (Ta = 25%, $V_{SS} = 0V$ , $C_L = 50pF$ )

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5		_	45	135	
Propagation Delay Time	10	t <sub>PLH</sub>	_	20	60	ns
	15		_	15	45	
	5			55	165	
Propagation Delay Time	10	$t_{ m PHL}$	_	25	75	ns
	15		_	20	60	
Input Capacitance		Cı	_		7.5	pF

1. Switching Time Test Circuit





## MN4082B/MN4082BS

## Dual 4-Input AND Gates

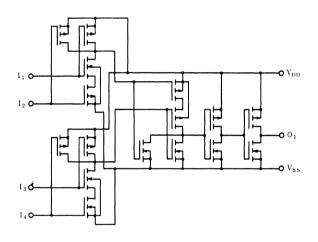
#### Description

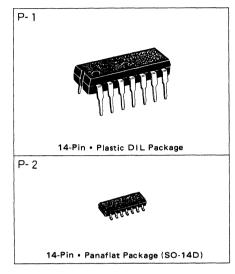
The MN4082B/S are dual 4-input AND gates.

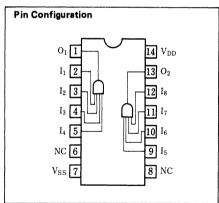
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

The MN4082B/S are equivalent to MOTOROLA MC14082B and RCA CD4082B.

#### Schematic Diagram (1/2)







### $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Itei	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	137
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperatur	e	Tstg	<b>−65∼+150</b>	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

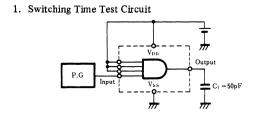


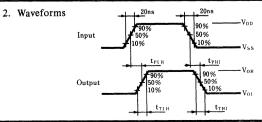
## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85℃</b>	Unit
nem	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0 :	5					1	_	1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{DD}$	_ ;	2	-	2		15	μA
	15				_	4	_	4	_	30	
	5		37 - 37	37	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or	$V_{ m DD}$	_	0.05		0.05		0.05	V
Bow Bever	15		$ I_{\rm O}  < 1\mu A$		_	0.05		0.05		0.05	
_	5		37 37	37	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	V DD	9.95		9.95		9,95		V
	15		$ I_{\rm O}  < 1\mu A$		14.95		14.95		14.95	-	
	5			Vo=0.5V or 4.5V	_	1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V
2011 20101	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4	-	4		4	
T 37 1	5			Vo=0.5V or 4.5V	3.5		3.5	_	3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$	7		7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11	_	
_	5		$V_0 = 0.4V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5V$	$V_I$ =0 or 10 $V$	1.3		1.1	_	0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6		3	_	2.4		
	5		$V_0 = 4.6 V$	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0$ or $10V$	1.3		1.1		0.9		mA
<u> </u>	15		$V_0 = 13.5V$	, V <sub>I</sub> =0 or 15V	3.6	***************************************	3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>I</sub> =0 or 15	5V		0.3		0.3		1	μA

## $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15		_	20	60	
	5		_	65	195	
Propagation Delay Time	10	t <sub>PLH</sub>	_	30	90	ns
	15		_	25	75	
	5		_	65	195	
Propagation Delay Time	10	t <sub>PHL</sub>	_	30	90	ns
	15		_	25	75	
Input Capacitance		Cı	_		7.5	pF





## MN4085B/MN4085BS

## Dual 2-Wide 2-Input AND-OR-Invert Gates

#### Description

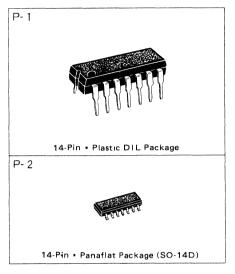
The MN4085B/S are dual 2-wide 2-input AND-OR-inverters. Their circuit is composed of two 2-input AND gates and a NOR gate.

Its logical expressions are

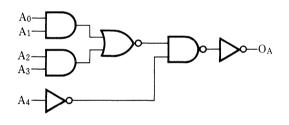
$$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$$
 $O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + A_4}$ 

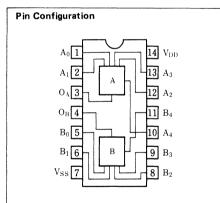
A High on the  $A_4$ ,  $B_4$  inputs inhibits the selecting action and force the outputs Low.

The MN4085B/S can be used where low power dissipation and high noise immunity is desired. The MN4085B is equivalent to RCA CD4085B.



#### Logic Diagram (1/2)





Ite	m	Symbol	Ratings	Unit	
Supply Voltage	Supply Voltage		-0.5∼+18	V	
Input Voltage		$V_{l}$	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_1$	max. 10	mA	
Power Dissipation	Ta=-40~+60°C	D	max. 400	117	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V



## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

TA	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	T 1
Item	(V)	bol		onaitions	min.	max.	min.	max.	min.	max.	Unit
Quiescent Power	5				_	1	_	1	_	7.5	
Supply Current	10	$I_{DD}$	$V_I = V_{SS or}$	$V_{DD}$	_	2	_	2		15	μA
- 11-7	15					4		4		30	
	5		V-V	37		0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	$\mathbf{v}_{\mathrm{DD}}$	_	0.05	_	0.05	_	0.05	V
2011 20101	15		$ 1_0  < 1\mu A$			0.05		0.05	_	0.05	
	5		V-V	17	4.95		4.95	_	4.95		
Gutput Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or	V DD	9.95		9.95		9.95	_	V
	15		$ I_0  < 1\mu A$		14.95		14.95	_	14.95	_	
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4		4	
Y	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			Vo=1.5V or 13.5V	11		11		11	_	
	5		$V_0 = 0.4V$	$V_I$ =0 or 5V	0.52	_	0.44		0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5V$	$V_i = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
20 11 20 101	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6V$	V <sub>i</sub> =0 or 5V	0.52		0.44	_	0.36	_	
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_I$ =0 or 10 $V$	1.3		1.1	_	0.9		mA
	15		Vo=13.5V	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV	_	0.3		0.3		1	μA

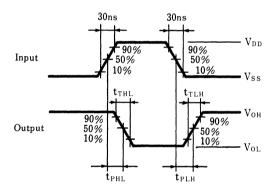
## 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15		_	20	60	
	5			65	195	
Propagation Delay Time	10	t <sub>PLH</sub>		30	90	ns
	15			20	60	
	5			75	225	
Propagation Delay Time	10	tPHL	_	30	90	ns
	15		_	20	60	
Input Capacitance		Cı	_	_	7.5	pF

- Switching Time Test Circuit and Waveform
  - 1. Measurement Condition

Test No.		Input Condition									
Test No.	A <sub>0</sub>	$A_1$	A <sub>2</sub>	A <sub>3</sub>	$A_4$						
1	P.G.	Н	L	L	L						
2	Н	P.G.	L	L	L						
3	L	L	P.G.	Н	L						
4	L	L	Н	P.G.	L						
5	P.G.	P.G.	P.G.	P.G.	L						
6	L	L	L	L	P.G.						

#### 2. Waveforms





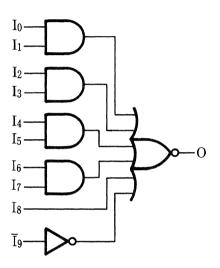
## MN4086B/MN4086BS

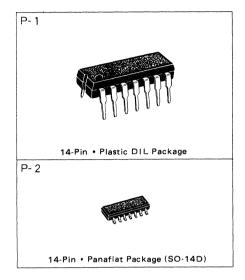
Expandable 4-Wide 2-Input AND-OR-Invert Gates

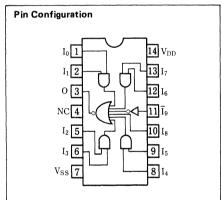
#### Description

The MN4086B/S are AND-OR select gates composed of four 2-input AND gates, an OR gate and an expansion input. Output can be obtained by inversion.

#### Logic Diagram







### **Maximum Ratings** $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5∼+18	V
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	337
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	P <sub>D</sub>	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	$^{\circ}$
Storage Temperature		Tstg	$-65 \sim +150$	ಭ

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

T4	$V_{\mathrm{DD}}$	Sym-		1 1:-:	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Y (
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	min.	max.	Unit
0:	5					1	_	1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I} = V_{SS}$ or	$ m V_{DD}$		2		2		15	$\mu$ A
	15					4	_	4	_	30	
_	5		V V	37	-	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	$v_{ m DD}$	_	0.05	_	0.05	-	0.05	V
	15		$ 1_0  < 1\mu A$		-	0.05	_	0.05	_	0.05	
0	5		$V_I = V_{SS}$ or	V	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_1 - V_{SS}$ or $ I_0  < 1\mu$ A	V DD	9.95		9.95		9.95	-	V
	15		$ 10  < 1\mu A$		14.95		14.95		14.95	-	
	5			Vo=0.5V or 4.5V		1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	-	3	-	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4	-	4	
T 37 14	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	-	V
	15			Vo=1.5V or 13.5V	11		11	_	11		
_	5		$V_0=0.4V$	$V_l = 0 \text{ or } 5V$	0.52	_	0.44	-	0.36		
Output Current Low Level	10	IoL	$V_0=0.5V$	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4	_	
	5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5V	0.52		0.44	****	0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
	15		Vo=13.5V	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	—Іон	$V_0=2.5V$	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV		0.3		0.3		1	μA

## $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_{L}\!=\!50pF)$

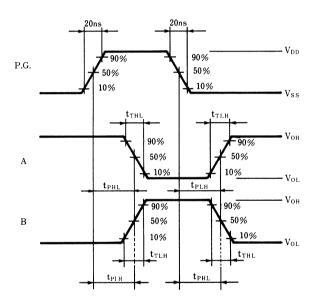
Owntening Onaracteristics	(1a 20 C,	V35 VV, C	L-Jupi /			
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	$t_{TLH}$		30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time	10	tTHL	_	30	90	ns
	15			20	60	
Propagation Delay Time	5			90	270	
$I_0 \sim I_7 \rightarrow O  (H \rightarrow L)$	10	t <sub>PHL</sub>	_	30	90	ns
	15			20	60	
Propagation Delay Time	5			80	240	
In $\sim$ I <sub>7</sub> $\rightarrow$ O (L $\rightarrow$ H)	10	t <sub>PLH</sub>		30	90	ns
10 -17 O (L11)	15			20	60	
Propagation Delay Time	5			70	210	
	10	$\mathbf{t}_{\mathtt{PHL}}$		25	75	ns
$I_8 \rightarrow O (H \rightarrow L)$	15		_	20	60	
Propagation Delay Time I <sub>8</sub> →O (L→H)	5		_	55	165	
	10	t <sub>PLH</sub>		20	60	ns
18-0 (L-n)	15			15	45	

## ■ Switching Characteristics $(Ta=25^{\circ}C, V_{SS}=0V, C_L=50pF)$ (Continued)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	55	165	
$\overline{I}_9 \rightarrow O (H \rightarrow L)$	10	tPHL		20	60	ns
19→O (H→L)	15			15	45	
Propagation Delay Time $\overline{I_9} \rightarrow O \ (L \rightarrow H)$	5		_	45	135	
	10	t <sub>PLH</sub>		15	45	ns
	15			10	30	
Input Capacitance		Cı			7.5	pF

#### • Dynamic Signal Waveforms

		Inp	ut Co	nditio	on	
	$I_0, I_1$	$I_2,I_3$	$I_{4}, I_{5}$	$I_{6}, I_{7}$	I <sub>8</sub>	Ī9
	P.G.	L	L	L	L	Н
	L	P.G.	L	L	L	Н
Α	L	L	P.G.	L	L	Н
	L	L	L	P.G.	L	Н
	L	L	L	L	P.G.	Н
В	L	L	L	L	L	P.G.



## MN4093B/MN4093BS

## Quad 2-Input NAND Schmitt Triggers

#### Description

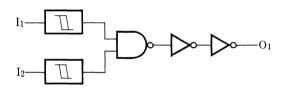
The MN4093B/S are quad 2-input NANDs with inputs which have the schmitt trigger function.

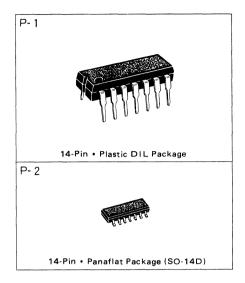
They are used for applications such as line drivers, reforming signals, multi-vibrators and so on because the two thresholds  $(V_{IH},\ V_{IL})$  are different for the rising and the falling edges of the input signal.

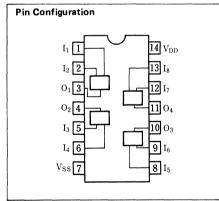
They have same pin outputs and may be replaced by the MN4011B.

The MN4093B/S are equivalent to MOTOROLA MC14093B and RCA CD4093B.

#### Schematic Diagram (1/4)







Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V	
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	337	
(per package)	Ta=+60~+85℃	$\mathbf{P}_{\mathtt{D}}$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

<sup>\*</sup> VDD + 0.5V should be under 18V



## $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Rein	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
	5					1		1	_	7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{DD}$	-	2	_	2	-	15	μA
11,	15					4		4	_	30	
	5		$V_{i}=V_{ssor}$	37	-	0.05	-	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1\mu$ A	V <sub>DD</sub>		0.05	_	0.05		0.05	V
20.1.21	15		$ 1_0  < 1\mu A$			0.05		0.05		0.05	
	5		$V_I = V_{SS}$ or	V	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_I - V_{SS}$ or $ I_O  < 1\mu A$	V DD	9.95		9.95		9.95	_	V
	15		10  \ 1 \mu A		14.95		14.95		14.95	_	
	5			Vo=0.5V or 4.5V		1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	$V_0=1V \text{ or } 9V$	_	3	_	3		3	V
Edit Edita	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
T 4 T7 14	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5		3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4 V$ ,	$V_I$ =0 or 5 $V$	0.52		0.44		0.36		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I$ =0 or 10V	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3	_	2.4		
0	5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5 $V$	0.52	_	0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4	_	
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV		0.3		0.3	_	1	μA

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

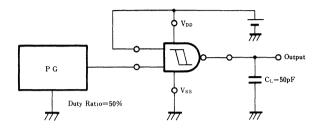
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time (Fig. 1)	10	$t_{\text{TLH}}$		30	90	ns
	15			20	60	
	5		Masser	60	180	
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>	-	30	90	ns
	15			20	60	
	5			85	255	
Propagation Delay Time (Fig. 1)	10	$t_{\scriptscriptstyle \mathrm{PLH}}$		40	120	ns
	15			30	90	
	5		_	90	270	
Propagation Delay Time (Fig. 1)	10	$t_{ m PHL}$		40	120	ns
	15			30	90	
	5			2.9	3.5	
Threshold Voltage (Fig. 2)	10	V <sub>IH</sub>		5.2	7	v
	15			7.3	11	
Threshold Voltage (Fig. 2)	5		1.5	2.2	_	
	10	$V_{IL}$	3	4.2	_	v
	15		4	6	_	

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Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Hysteresis Voltage (Fig. 2)	5		0.4	0.7		
	10	V <sub>H</sub>	0.6	1		v
	15		0.7	1.3		
Input Capacitance		CI		_	7.5	pF

Fig. 1 Switching Time Test Circuit and Waveforms

#### 1. Test Circuit



#### 2. Waveforms

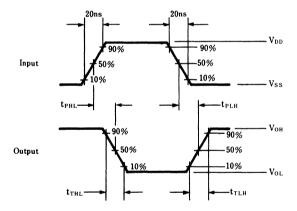
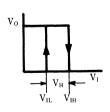
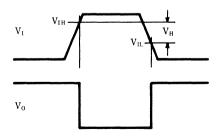


Fig. 2 Transfer Characteristics



Transfer Characteristics



The upper waveform shows its definition rating 30%, to 70% limit

# MN4094B/MN4094BS

8-Stage Shift- and -Store Bus Registers

#### Description

The MN4094B/S are shift-and-store bus registers composed of an 8-bit shift register and an 8-bit latch.

The data read-in to the shift register can be taken into the latch by asynchronous strobe input, and output can be held in the data transfer mode.

Directly connected to an 8-bit bus line since the parallel output is 3-state construction.

They are suitable for series-parallel converters and data receivers. ceiver.

#### Truth Table

	Inj	put		Parallel	Output	Serial	Output
CP	EO	STR	D	Oo	On	Os	O's
	L	×	×	Z	Z	O <sub>6</sub> ′	nc
~	L	×	×	Z	Z	nc	O <sub>7</sub>
	Н	L	×	nc	nc	O <sub>6</sub> ′	nc
	Н	Н	L	L	$O_{n-1}$	$O_6'$	nc
	Н	Н	Н	Н	$O_{n-1}$	O <sub>6</sub> ′	nc
~	Н	Н	Н	nc	nc	nc	O <sub>7</sub>

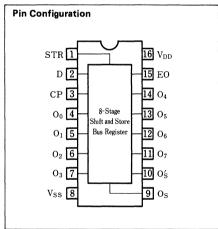
Note)

X : don't careZ : high impedance

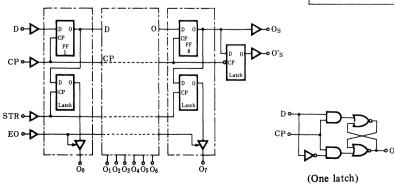
nc: no change

O'<sub>6</sub>: 7-stage shift register mode

# P- 3 16-Pin • Plastic DIL Package P- 4 16-Pin • Panaflat Package (SO-16D)



## Logic Diagram



# ■ Maximum Ratings (Ta=25°C)

Item		Symbol	Ratings	Unit	
Supply Voltage	oltage		$-0.5 \sim +18$	V	
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output (	Current	$\pm I_{I}$	max. 10	mA	
Power Dissipation	Γa=-40~+60°C		max. 400	117	
(per package)	Γa=+60~+85°C	$P_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (pe	r output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	Ĉ	
Storage Temperature		Tstg	-65~+150	°C	

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

*.	$V_{DD}$	Sym-		7	Ta=-	-40℃	Ta=	25℃	Ta=85℃		Unit
Item	(V)	bol	(	Conditions		max.	min.	max.	min.	max.	Unit
Quiescent Power	5				_	20	_	20	_	150	
Supply Current	10	$I_{\mathrm{DD}}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$	—	40		40	-	300	μA
	15					80	_	80		600	
0 ( ) 17 1	5		$V_I = V_{SS}$ or	·V		0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1 \mu A$	VDD	_	0.05	_	0.05	_	0.05	V
	15		10  \ 1 \mu A			0.05		0.05		0.05	
0 4 4 77 14	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95	_	4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1 \mu A$	VDD	9.95		9.95		9.95	_	V
	15		10  \ 1μΛ		14.95		14.95		14.95		
Y 4 X7 14	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	_	1.5		1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3	_	3		3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
Input Voltage	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5		3,5		
High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7	_	7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11	_	
0 1 10 1	5		$V_0=0.4V$	$V_l = 0 \text{ or } 5V$	0.52		0.44		0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
-	15		$V_0 = 1.5 V_1$	$V_l = 0$ or $15V$	3.6		3		2.4		
Outros Comment	5		$V_0 = 4.6V$	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1	_	0.9	-	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	$\pm I_I$	$V_{I} = 0 \text{ or } 19$	5V		0.3		0.3		1	μA
3-State Leakage Current High Leve	15	$I_{OZH}$	$V_0 = V_{DD}$		_	1.6		1.6		12	μA
Output Pin Leakage Current Low Leve	15	$-I_{ozL}$	$V_o = V_{ss}$			1.6	_	1.6	_	12	μπ

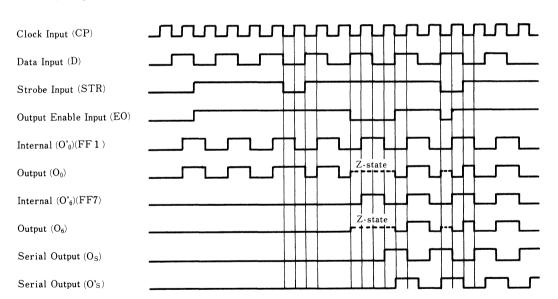


Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15		_	20	60	
	5		_	135	405	
Propagation Delay Time	10	t <sub>PHL</sub>		65	195	ns
$CP \rightarrow Os (H \rightarrow L)$	15			50	150	
	5		_	105	315	
Propagation Delay Time	10	t <sub>PLH</sub>	_	50	150	ns
$CP \rightarrow Os (L \rightarrow H)$	15	12		40	120	
D 1 m	5			105	315	
Propagation Delay Time	10	t <sub>PHL</sub>	_	50	150	ns
$MR \rightarrow O$ 's $(H \rightarrow L)$	15	1116	_	40	120	
	5			105	315	<u> </u>
Propagation Delay Time	10	t <sub>PLH</sub>	_	50	150	ns
MR→O's (L→H)	15	VFLH	_	40	120	
	5			165	495	
Propagation Delay Time	10	$t_{ ext{PHL}}$	_	75	225	ns
$CP \rightarrow On (H \rightarrow L)$	15	CPAL		55	165	
	5			150	450	
Propagation Delay Time	10	t		70	210	ns
$CP \rightarrow On (L \rightarrow H)$	15	t <sub>PLH</sub>	_	55	165	115
	5			110	330	
Propagation Delay Time	10			50	150	
STR→On (H→L)	15	$t_{ ext{PHL}}$	_	35	105	ns
	5			100	300	
Propagation Delay Time			_	45	l	
$STR \rightarrow On (L \rightarrow H)$	10	$\mathbf{t}_{\mathtt{PLH}}$		1	135	ns
	15	<del> </del>		35	105	
High Level Output Disable Time	5		_	75	225	
EO→On (H)	10	t <sub>PHZ</sub>		40	120	ns
	15			30	90	
Low Level Output Disable Time	5		_	80	240	
EO→On (L)	10	t <sub>PLZ</sub>		40	120	ns
	15			30	90	ļ
High Level Output Enable Time	5		_	40	120	
EO→On (H)	10	$t_{PZH}$	_	25	75	ns
	15	1		20	60	-
Low Level Output Enable Time	5		_	40	120	
EO→On (L)	10	$t_{PZL}$	_	25	75	ns
	15	1		20	60	-
Set-up Time	5		_	30	90	
D→CP	10	tsu	_	10	30	ns
	15			5	15	

# Switching Characteristics ( $Ta = 25^{\circ}C$ , $V_{SS} = 0V$ , $C_1 = 50pF$ ) (continued)

Item	$V_{DD}(V)$	Symbol	mın.	typ.	max.	Unit
Hold Time	5			-15	5	
D→CP	10	$t_{hold}$	_	5	20	ns
	15			5	20	
	5		and the same of th	20	90	
Minimum Clock Pulse Width	10	twcpl		15	45	ns
	15			12	36	
	5		_	20	60	
Minimum Strobe Pulse Width	10	twstrh	_	15	45	ns
	15			12	36	
	5		5	10		
Maximum Clock Frequency	10	fmax	11	22	_	MHz
	15		14	28	_	
Input Capacitance		Cı	_		7.5	pF

## ■ Timing Diagram



# MN4502B/MN4502BS

# Hex Strobed Inverting Buffers

## Description

The MN4502B/S are 3-state output inverting buffers with a strobe terminal, and can drive 1 TTL in the 74 series.

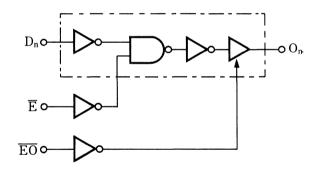
#### Truth Table

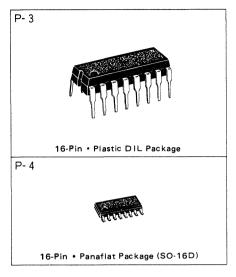
	Input		Output
$D_n$	Ē	ĒΟ	O <sub>n</sub>
L	L	L	Н
Н	L	L	L
×	Н	L	L
×	×	Н	Z

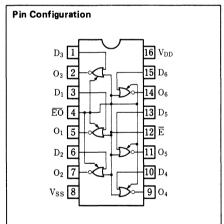
Note)

X: don't care Z: high impedance

## Logic Diagram (1/6)







#### Maximum Ratings $(T_a=25^{\circ})$

Ite	m	Symbol	Ratings	Unit		
Supply Voltage	Supply Voltage		-0.5~+18	V		
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V		
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V		
Input Current	nput Current		ut Current		max. 10	mA
Output Current		$\pm I_{\rm I}$	max. 30	mA		
Power Dissipation (per package)	$T_a = -40 \sim +60 ^{\circ} \text{C}$ $T_a = +60 \sim +85 ^{\circ} \text{C}$	$P_D$	max. 400  Decrease up to 200mW rating at 8mW/°C	mW		
Power Dissipation (	per output terminal)	P <sub>D</sub>	max. 100	mW		
Operating Ambient Temperature		Topr	<b>−40~+85</b>	°C		
Storage Temperatur	Storage Temperature		<b>−65</b> ~+150	°C		

\* VDD + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	V <sub>DD</sub>	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Ta=	<b>25℃</b>	Ta=	<b>85</b> ℃	Timia
ntem	(V)	bol		Conditions		max.	min.	max.	min.	max.	Unit
O :	5					4	_	4	_	30	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	8	_	8		60	μA
	15					16	_	16	_	120	
	5.		$V_{i}=V_{SS}$ or	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1\mu$ A	V <sub>DD</sub>	_	0.05	-	0.05	_	0.05	V
	15		1 <sub>0</sub>   < 1μΑ		_	0.05	_	0.05	_	0.05	
	5		$V_I = V_{SSOr}$	V -	4.95		4.95	-	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$ V_1 - V_{SS} O \Gamma $ $ I_0  < 1 \mu A$	v DD	9.95	_	9.95	_	9.95	_	V
	15		10  < 1μA	$ I_0  < I \mu A$			14.95		14.95		
	5			Vo=0.5V or 4.5V		1.5	_	1.5	-	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	_	3	-	3	v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4	_	4		4	
Torres 4 37 - 14	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7	_	7	_	V
	15			Vo=1.5V or 13.5V	11	_	11		11		
	4.75		$V_0 = 0.4V$	$V_I = 0$ or $5V$	3.5		2.9	_	2.3		
Output Current Low Level	10	IoL	$V_0 = 0.5V$	$V_I$ =0 or 10 $V$	12	_	10	_	8		mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	24		20		16		
	5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5 $V$	1.2		1	_	0.8		
Output Current High Level	10	—I <sub>он</sub>	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	3.8		3.2	_	2.5		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	12		10		8		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	3.8		3.2		2.5		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	5V	_	0.3		0.3		1	μA
3-State Leakage Current High Leve	15	Iozh	$V_0 = V_{DD}$		_	1.6	_	1.6		12	μA
Output Pin Leakage Current Low Leve	15	-I <sub>ozL</sub>	$V_0 = V_{SS}$		_	1.6		1.6		12	μΑ

# $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	30	90	
Output Rise Time	10	t <sub>TLH</sub>	_	15	45	ns
	15		_	12	36	
	5		_	25	75	
Output Fall Time	10	t <sub>THL</sub>		12	36	ns
	15		_	8	24	
Propagation Delay Time	5		_	85	255	
Dn. Ē→On (H→L)	10	$t_{ ext{PHL}}$		40	120	ns
Dii, E-Oii (II-E)	15			35	105	
Propagation Delay Time	5		_	80	240	
Dn, Ē→On (L→H)	10	$t_{\mathrm{PLH}}$	_	35	105	ns
Dii, E-Oii (E-II)	15		_	30	90	
High Level Output Disable Time  EO→On (H)	5		_	60	180	
	10	t <sub>PHZ</sub>	_	55	165	ns
EO-Oii (II)	15			55	165	

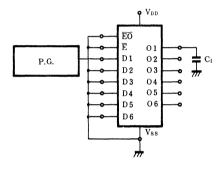


Switching Characteristics ( $Ta = 25^{\circ}C$ , $V_{SS} = 0V$ , $C$
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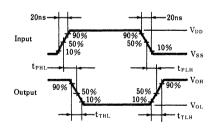
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Low Level Output Disable Time $\overline{EO} \rightarrow On  (L)$	5		_	50	150	
	10	t <sub>PLZ</sub>		35	105	ns
	15		<del></del>	30	90	
High Level Output Enable Time	5		_	60	180	
	10	t <sub>PZH</sub>	_	35	105	ns
<del>EO</del> →On (H)	15			30	90	
Low Level Output Enable Time	5		_	55	165	
EO→On (L)	10	tPZL	_	25	75	ns
	15			20	60	
Input Capacitance		C <sub>I</sub>	_		7.5	pF

## • Switching Time Test Circuit and Waveforms

#### 1. Test Circuit



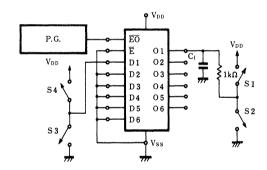
#### 2. Waveforms



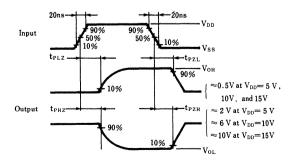
#### • 3-State Test Circuit and Waveforms

TEST	S1	S2	S3	S4
$t_{\mathrm{PHZ}}$	Open	Closed	Closed	Open
$t_{PLZ}$	Closed	Open	Open	Closed
$\mathbf{t}_{ ext{PZL}}$	Closed	Open	Open	Closed
$t_{\mathtt{PZH}}$	Open	Closed	Closed	Open

#### 1. Test Circuit



#### 2. Waveforms



# MN4503B/MN4503BS

Hex Non-Inverting 3-State Buffers

#### Description

The MN4503B/S are non-inverting tristate buffers which have a high current source and sink capability. There are two disable inputs (EO<sub>2</sub>, EO<sub>4</sub>) which enable control of 2 or 4 circuits independently. A High on the EO<sub>4</sub> makes outputs 1 through 4 High impedance, and the EO<sub>2</sub> makes outputs 5, 6 High impedance.

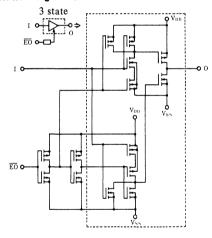
MN4503B/S are equivalent to MOTOROLA MC14503B.

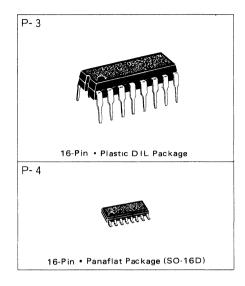
#### Truth Table

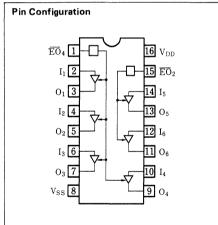
In	put	Output			
I	ĒΟ	0			
L	L	L			
Н	L	Н			
×	Н	Z			

Note) X: don't care; Z: high impedance (OFF mode)

## Schematic Diagram (3 state 1/6)







#### ■ Maximum Ratings (Ta=25°C)

Ite	em	Symbol	Ratings	Unit		
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V		
Input Voltage		VI	$-0.5 \sim V_{DD} + 0.5^*$	V		
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V		
Peak Input · Outpu	t Current	$\pm  I_I$	max. 25	mA		
Power Dissipation	Ta=-40~+60°C	D	max. 400	117		
(per package)	Ta=+60~+85°C	$\mathrm{P}_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW		
Power Dissipation (	per output terminal)	$P_{\mathrm{D}}$	max. 100	mW		
Operating Ambient Temperature Topr			-40~+85	°C		
Storage Temperatu	re	Tstg	$-65 \sim +150$	°C		

<sup>\*</sup> VDD + 0.5V should be under 18V



# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

***************************************	T.4	$V_{ m DD}$	Sym-		3 1141	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	11
	Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
		5				_	4	_	4	_	30	
	ent Power Current	10	$I_{DD}$	$V_I = V_{SS or}$	$V_{DD}$		8	_	8		60	$\mu$ A
		15					16	_	16	_	120	
•		5		$V_I = V_{SS}$ or	V		0.05	_	0.05		0.05	
Low L	t Voltage evel	10	Vol	$ I_{\rm O}  < 1\mu A$	VDD	_	0.05	_	0.05		0.05	V
		15		10  < 1µA		_	0.05	_	0.05		0.05	
0	. 77 1.	5		$V_i = V_{ssor}$	Van	4.95		4.95		4.95	_	
High L	t Voltage .evel	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	עט י	9.95		9.95		9.95	-	V
		15		10  \ 1 \mu \		14.95		14.95		14.95		
Input Voltage Low Level	5			Vo=0.5V or 4.5V	_	1.5	_	1.5	_	1.5		
	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V	
		15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Immus 1	V-lt	5		$ I_0  < 1\mu A$	$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5	_	3.5		3.5	_	
High L	Voltage .evel	10	VIH		V <sub>0</sub> =1V or 9V	7	_	7	annua.	7		V
_		15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	_	4.75		$V_0=0.4V$	$V_I = 0$ or $5V$	1.7		1.4		1.1		
Output Low L	t Current evel	10	IoL	$V_0=0.5V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	4.8		4	_	3.2	_	mA
		15		$V_0 = 1.5V$ ,	$V_I$ =0 or 15 $V$	12		10		8		
_		5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5 $V$	1		0.88	_	0.7		
Outpu High L	t Current evel	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10 $V$	2.4		2.2	_	1.8	_	mA
		15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	6.6		6		4.8		
Output C	Current High Level	5	-Іон	$V_0 = 2.5 V$ ,	$V_0$ =2.5V, $V_I$ =0 or 5V			1.4		1.1		mA
Input Le	eakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 19	5V		0.3		0.3		1	μA
3-State	Leakage Current High Level	15	I <sub>OZH</sub>	$V_0 = V_{DD}$		_	1.6		1.6		12	μA
Output Pin	Leakage Current Low Level	15	$-I_{OZL}$	$V_0 = V_{SS}$		_	1.6		1.6		12	μΛ.

# $\blacksquare$ Switching Characteristics $(Ta\!=\!25\mbox{°C}$ , $V_{\rm SS}\!=\!0\,V,~C_L\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5			35	105		
Output Rise Time (Fig. 1)	10	t <sub>TLH</sub>		20	60	ns	
	15			15	45		
	5		-	30	90		
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>	_	15	45	ns	
	15		_	10	30		
	5			60	180		
Propagation Delay Time (Fig. 1)	10	$t_{\scriptscriptstyle \mathrm{PLH}}$		25	75	ns	
	15			20	60		
	5		_	70	210	ns	
Propagation Delay Time (Fig. 1)	10	$\mathbf{t}_{\mathtt{PHL}}$	_	30	90		
	15		_	25	75		
	5			45	135		
3-State Propagation Delay Time O (H) → High Impedance (Fig. 2)	10	t <sub>PHZ</sub>		35	105	ns	
(11) 111gii Impoduitoo (11g. 2)	15		_	30	90		
	5			60	180		
3-State Propagation Delay Time O(L) → High Impedance (Fig. 3)	10	t <sub>PLZ</sub>		35	105	ns	
C(L) - Ingli impedance (Fig. 3)	15		_	25	75		

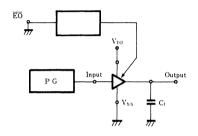
# ■ Switching Characteristics $(Ta=25\%, V_{SS}=0V, C_L=50pF)$ (continued)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5			75	225		
3-State Propagation Delay Time High Impedance → O (H) (Fig. 2)	10	t <sub>PZH</sub>		35	105	ns	
	15						90
	5			95	285		
3-State Propagation Delay Time High Impedance → O (L)(Fig. 3)	10	t <sub>PZL</sub>		40	120	ns	
right impedance / O (L)(Fig. 3)	15		_	30	90		
Imput Capacitance		CI	_	_	7.5	pF	

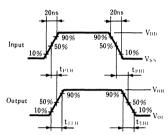
## • Switching Time Test Circuit and Waveforms

(Fig. 1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}$ ,  $t_{PHL}$ 

## 1. Test Circuit

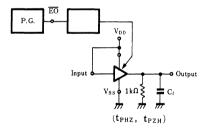


2. Waveforms

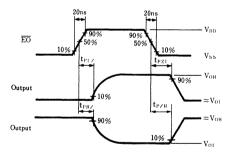


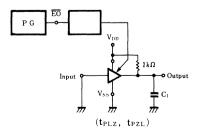
(Fig. 2)  $t_{\text{PHZ}}\,,\ t_{\text{PZH}}\,,\ t_{\text{PLZ}}\,,\ t_{\text{PZL}}$ 

#### 1. Test Circuit



# 2. Waveforms







# MN4510B/MN4510BS

# BCD Up/Down Counters

#### Description

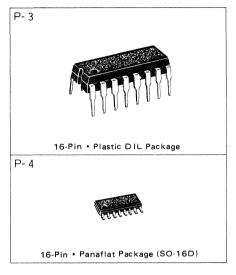
The MN4510B/S are BCD up/down counters composed of a gate circuit with the function of D-flip-flop 4-stage and T-flip-flop. The counter is cleared when MR is "H". High speed operation is possible due to internal synchronization.

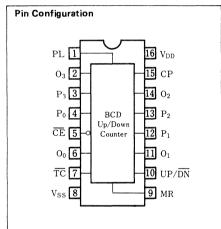
The MN4510B/S are suitable for up/down counters, frequency synthesizers which need low power dissipation and high noise immunity, and also for A/D and D/A converters.

They are equivalent to MOTOROLA MC14510B and RCA CD4510B.

#### Truth Table

MR	PL	UP/DN	ĈĒ	CP	Mode
L	Н	×	×	×	load
L	L	×	Н	×	no change
L	L	L	L		count down
L	L	Н	L		count up
Н	×	×	×	×	leset





#### Maximum Ratings (Ta=25°C)

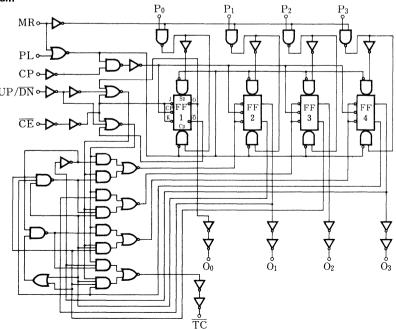
Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	$-0.5 \sim +18$	V
Input Voltage		$V_{\rm I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{0}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	11.
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{\mathrm{D}}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> VDD + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Ta=	25℃	Ta=	85℃	** **
	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
	5					20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or		40	_	40		300	μA	
	15					80	_	80	_	600	
	5		V – V	V		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	V <sub>DD</sub>		0.05	_	0.05		0.05	V
Eow Ecrei	15		$ 1_0  < 1\mu A$			0.05		0.05		0.05	
	5		V - V	3.7	4.95	_	4.95		4.95		
Output Voltage High Level	10	Voh	$V_I = V_{SS}$ or $ I_O  < 1 \mu A$	$V_{\mathrm{DD}}$	9.95		9.95		9.95		V
	15		$ 1_0  < 1 \mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3		3	V
2011 221 12	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Y	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7	_	7		V
	15			Vo=1.5V or 13.5V	11	-	11		11		
	5		$V_O = 0.4V$	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I {=} 0 \ or \ 10 \mathrm{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6		3		2.4		
	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44	-	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3		1.1		0.9	_	mA
mgn Bever	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	V <sub>i</sub> =0 or 15	SV		0.3	_	0.3		1	μA

# Logic Diagram





■ Switching Characteristics  $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$ 

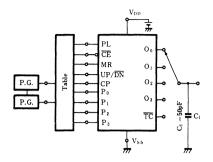
Item	$V_{\mathrm{DD}}\left( \mathrm{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Decreasion Delev Time	5		_	145	435	
Propagation Delay Time	10	t <sub>PHL</sub>	_	60	180	ns
$CP \rightarrow On (H \rightarrow L)$	15		_	45	135	
D	5			155	465	
Propagation Delay Time	10	t <sub>PLH</sub>		65	195	ns
$CP \rightarrow On (L \rightarrow H)$	15	1 1 1 1 1	_	45	135	
D .: D1 T'	5		_	260	780	
Propagation Delay Time	10	t <sub>PHI</sub>		105	315	ns
$CP \rightarrow \overline{TC} (H \rightarrow L)$	15	, or mi		75	225	
	5			180	540	
Propagation Delay Time	10	tPLH		75	225	ns
$CP \rightarrow \overline{TC} (L \rightarrow H)$	15	CP1.H		55	165	5
	5			125	375	
Propagation Delay Time	10	+		55	165	ns
$PL \rightarrow On (H \rightarrow L)$	15	t <sub>PHL</sub>		40	120	115
	5	1				
Propagation Delay Time	1			170	510	
$PL \rightarrow On (L \rightarrow H)$	10	t <sub>PLH</sub>	_	70	210	ns
	15			50	150	
Propagation Delay Time	5			250	750	
$PL \rightarrow \overline{TC} (H \rightarrow L)$	10	t <sub>PHL</sub>		110	330	ns
	15			80	240	
Propagation Delay Time	5		_	250	750	
$PL \rightarrow \overline{TC} (L \rightarrow H)$	10	t <sub>PLH</sub>	_	110	330	ns
	15			80	240	
Propagation Delay Time	5		_	165	495	
$\overline{CE} \rightarrow \overline{TC} (H \rightarrow L)$	10	t <sub>PHL</sub>	_	65	195	ns
	15			50	150	
Propagation Delay Time	5		_	145	435	
$\overline{CE} \rightarrow \overline{TC} (L \rightarrow H)$	10	t <sub>PLH</sub>	- Marine	60	180	ns
	15			45	135	
Propagation Delay Time	5		_	205	615	
MR→On, TC (H→L)	10	t <sub>PHL</sub>	_	65	195	ns
On, 10 (11 °L)	15		_	45	135	
Propagation Delay Time	5			225	675	
	10	$t_{\rm PLH}$		75	225	ns
$MR \rightarrow \overline{TC} (L \rightarrow H)$	15			50	150	
	5		_	45	135	
Minimum Clock Pulse Width	10	t <sub>WCPL</sub>	_	20	60	ns
	15		_	15	45	

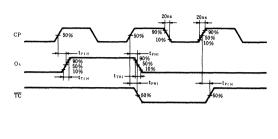
# **CMOS Logic MN4000B Series**

Switching Characteristics	(1a-25)	vss-uv, c	7 L — 30 pr / (	onthiuca)		
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	55	165	
Minimum PL Pulse Width	10	twPLH	_	25	75	ns
	15		_	15	45	
	5		_	60	180	
Minimum Reset Pulse Width	10	twmRH	_	25	75	ns
	15		_	20	60	
	5			65	195	
Reset Recovery Time	10	t <sub>RMR</sub>	_	20	60	ns
	15		_	15	45	
	5		_	75	225	
PL Recovery Time	10	t <sub>RPL</sub>	_	25	75	ns
	15		_	15	45	
Set-up Time	5		_	50	150	
=	10	tsu		25	75	ns
Pn→PL	15		-	20	60	
Set-up Time UP/ <del>DN</del> →CP	5		_	125	375	
	10	tsu	-	50	150	ns
UP/DN→CP	15			35	105	
Set-up Time	5		_	60	180	
Secup Time <del>CE</del> →CP	10	tsu	_	20	60	ns
CE→CF	15	}	_	10	30	
Hold Time	5	i i	_	-40	10	
Pn→PL	10	thold		-20	5	ns
rn→r∟	15			-20	0	}
Hold Time	5			-90	35	
Hold Time UP/DN→CP	10	thold	_	-35	15	ns
OF/DN-CF	15		_	-25	15	
Hold Time	5		_	-40	20	
Time <del>CE</del> →CP	10	thold	_	-15	5	ns
CE→CF	15			-10	5	
	5		5	10	_	
Maximum Clock Frequency	10	fmax	12	24	_	MHz
	15		17	34	_	
Input Capacitance		Cı	_	_	7.5	pF

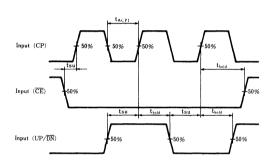


- Switching Time Test Circuit and Waveforms
  - 1. Test Circuit

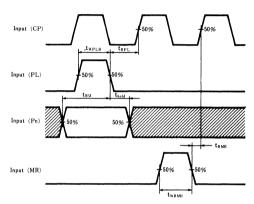




2. Waveforms

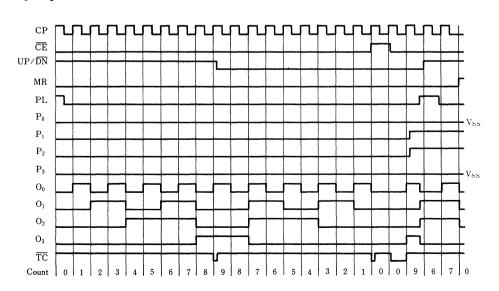


Waveforms showing minimum pulse width for CP, set-up and hold times for  $\overline{CE}$  to CP and UP/ $\overline{DN}$  to CP



Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for Pn to PL

#### Timing Diagram



# MN4511B/MN4511BS

BCD-to-7-Segment Decoder/Drivers

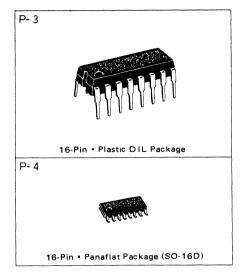
#### Description

The MN4511B/S are decoder/drivers which convert from 4-bit latch and 4-bit BCD code input to 7-segment output.

Features are lamp test input (LT) for display tests, blanking input (BI) to adjust turn-off at pulse drive and brightness, and latch enable input (EL) to latch BCD input tentatively.

Output is obtained by driving directly or through driver element LED, LCD and fluorescent lamp since an NPN bipolar transistor and N-channel MOS transistor are connected complementarily. Application examples are measuring equipment, clocks and timers.

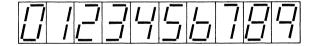
They are equivalent to MOTOROLA MC14511B.

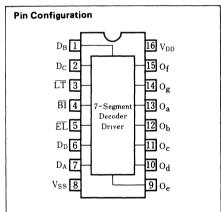


#### Segment Configuration



#### Display





## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^{*1}$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^{*1}$	V	
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA	
Power Dissipation	Ta=-40~+60°C	D	max. 400	mW	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	n w	
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Maximum Output I	Oriving Current	I OH max	25	mA	
Maximum Output I	t Power*2 PoH max.		50	mW	
Operating Ambient	Temperature	Topr	-40~+85	$^{\circ}$	
Storage Temperatur	re	Tstg	-65~+150	°C	

\* 2  $P_{OH max} = I_{OH} (V_{DD} - V_{OH})$ \* 1 V<sub>DD</sub>+0.5V should be under 18V





# $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=25℃		Ta=	85℃	Unit
	(V)	bol	·	onaitions	min.	max.	min.	max.	min.	max.	Unit
0.1	5				_	20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$	_	40	_	40	_	300	μA
	15					80	_	80	_	600	
_	5		V-V	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	V <sub>DD</sub>		0.05		0.05	_	0.05	v
	15		$ 10  < 1\mu A$			0.05	_	0.05		0.05	
Onton M. I.	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95		4.95		4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	V <sub>DD</sub>	9.95	_	9.95	_	9.95		V
	15		1 <sub>0</sub>   < 1μΑ		14.95		14.95		14.95		
* . ** 1.	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	Vil	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4	_	4	_	4	
Immut Walters	5			Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5	_	
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7	_	7	_	V
	15			Vo=1.5V or 13.5V	11		11		11	_	
	5		$V_0=0.4V$	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5 V$	$V_I$ =0 or 10V	1.3	_	1.1	_	0.9	_	mA
	15		$V_0 = 1.5 V$	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Input Leakage Current	15	$\pm I_I$	$V_{\rm i} = 0 \text{ or } 15$	SV .		0.3	_	0.3	_	1	μA

# $\blacksquare$ DC Characteristics $(V_{SS} {=} 0V)$

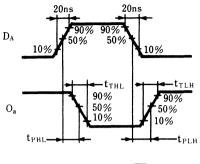
Item	$V_{ m DD}$	Sym-	Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	Conditions	min.	max.	min.	max.	min.	max.	Unit
	5			4.10		4.10	4.40	4.10	_	
	10	V <sub>OH</sub>	I <sub>OH</sub> =0 <sub>m</sub> A	9.10	_	9.10	9.40	9.10	_	V
	15			14.10		14.10	14.40	14.10		
	5					_	4.30	_		
	10	VoH	I <sub>OH</sub> =5mA	_		_	9.30	-	_	V
	15					_	14.30		_	
	5			3.60		3.60	4.25	3.30		
	10	VoH	I <sub>OH</sub> =10mA	8.75	_	8.75	9.25	8.45	-	V
Output Driving	15			13.75		13.75	14.25	13.45		
Voltage	5			_	_		4.20			
	10	Von	I <sub>OH</sub> =15mA	-			9.20	_	_	V
	15			_		_	14.20	_		
	5			2.80	_	2.80	4.20	2.50	_	
	10	Von	I <sub>OH</sub> =20mA	8.10	-	8.10	9.20	7.80	_	V
	15			13.10		13.10	14.20	12.80	_	
	5			_		_	4.15	_	_	
	10	Von	I <sub>OH</sub> =25mA	_	-	_	9.20	_	_	V
	15						14.20			

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	18	54	
Output Rise Time (Fig. 1)	10	t <sub>TLH</sub>		11	33	ns
-	15			9	27	
	5		_	60	180	
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>		30	90	ns
•	15		_	20	60	
(Fig. 1)	5		_	155	465	
Propagation Delay Time (Fig. 1)	10	$t_{ ext{PHL}}$		60	180	ns
$Dn \rightarrow On (H \rightarrow L)$	15		_	40	120	
(Fig. 1)	5			135	405	
Propagation Delay Time (Fig. 1)	10	t <sub>PLH</sub>	_	55	165	ns
$Dn \rightarrow On (L \rightarrow H)$	15		_	40	120	
(Fig. 2)	5		_	160	480	
Propagation Delay Time (Fig. 2)	10	tpHL	_	60	180	ns
$\overline{EL} \rightarrow On \ (H \rightarrow L)$	15	1	_	45	135	
(Fig. 2)	5		_	160	480	<del> </del>
Propagation Delay Time (Fig. 2)	10	tplH		60	180	ns
$\overline{\mathrm{EL}} \rightarrow \mathrm{On} \ (\mathrm{L} \rightarrow \mathrm{H})$	15		_	45	135	
- (Fig 3)	5		_	120	360	
Propagation Delay Time (Fig. 3)	10	t <sub>PHL</sub>		50	150	ns
$\overline{\mathrm{BI}} \rightarrow \mathrm{On} \ (\mathrm{H} \rightarrow \mathrm{L})$	15	12		35	105	
(Fig. 3)	5		_	105	315	
Propagation Delay Time (Fig. 3)	10	tplH	_	40	120	ns
$\overline{\text{BI}} \rightarrow \text{On} \ (L \rightarrow H)$	15	1	_	30	90	
Propagation Delay Time (Fig. 4)	5		_	65	195	
	10	t <sub>PHL</sub>	_	25	<b>.</b> 75	ns
$\overline{LT} \rightarrow On (H \rightarrow L)$	15			20	60	
Fig 4)	5			50	150	
Propagation Delay Time (Fig. 4)	10	t <sub>PLH</sub>	_	25	75	ns
$LT \rightarrow On (L \rightarrow H)$	15		_	20	60	
(7)	5		_	25	75	
Minimum EL Pulse (Fig. 2) Width	10	twell	_	10	30	ns
Width	15		_	8	24	
- (Fig 2)	5		_	15	45	
Set-up Time (Fig. 2)	10	tsu		5	15	ns
Dn→EL	15		_	5	15	
(Fig. 2)	5			10	30	
Hold Time (Fig. 2)	10	thold	_	5	15	ns
Dn→ĒĹ	15		_	5	15	
Input Capacitance		Cı	_	-	7.5	pF
	l	1	L		L	<u> </u>

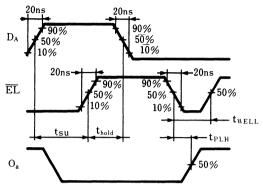


#### • Dynamic Signal Waveforms

(Fig. 1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PHL}$  ( $Dn \rightarrow On$ ),  $t_{PLH}(Dn \rightarrow On)$  (Fig. 2)  $t_{PHL}(\overline{EL} \rightarrow On)$ ,  $t_{PLH}(\overline{EL} \rightarrow On)$ ,  $t_{WELL}$ ,  $t_{SU}$ ,  $t_{hold}$ 

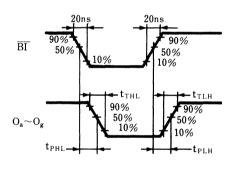


Input  $D_B$ ,  $D_C$ ,  $D_D$  and  $\overline{EL} = "L"$ Input  $\overline{BI}$  and  $\overline{LT}$  = "H"



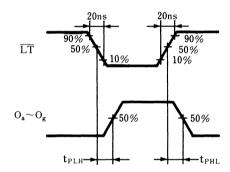
Input DB, Dc and DD= "L" Input  $\overline{BI}$  and  $\overline{LT}$ = "H"

(Fig. 3) 
$$t_{PHL}(\overline{BI} \rightarrow On)$$
,  $t_{PLH}(\overline{BI} \rightarrow On)$ 



Input  $D_A$ ,  $D_B$ ,  $D_C$  and  $\overline{EL} =$  "L" Input  $D_D$  and  $\overline{LT}$  = "L"

# (Fig. 4) $t_{PHL}(\overline{LT} \rightarrow On)$ , $t_{PLH}(\overline{LT} \rightarrow On)$



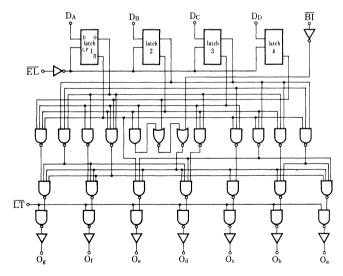
Input  $D_A$ ,  $D_B$  and  $\overline{EL} = "L"$ Input Dc, DD and BI= "H"

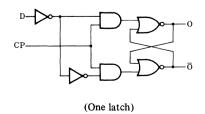
# Truth Table

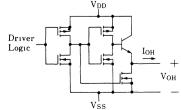
			Input				Output							Display
EL	BĪ	ĪΤ	Dъ	Dc	Dв	Da	Oa	Ob	Oc	Od	Oe	Of	Og	Display
×	×	L	×	×	×	×	Н	Н	Н	Н	Н	Н	Н	8
×	L	Н	×	×	×	X	L	L	L	L	L	L	L	blank
L	Н	H	L	L	L	L	Н	Н	Н	Н	Н	Н	,L	0
L	Н	Н	L	L	L	Н	L	Н	Н	L	L	L	L	1
L	Н	Н	L	L	Н	L	Н	Н	L	Н	Н	L	Н	2
L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
L	Н	Н	L	Н	L	L	L	Н	Н	L	L	Н	Н	4
L	Н	Н	L	Н	L	Н	Н	L	Н	Н	L	Н	Н	5
L	Н	Н	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	6
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
L	Н	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
L	Н	Н	Н	L	L	Н	Н	Н	Н	L	L	H	Н	9
L	Н	Н	Н	L	Н	L	L	L	L	L	L	L	L	blank
L	Н	Н	Н	L	Н	Н	L	L	L	L	L	L	L	blank
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	blank
L	Н	Н	Н	Н	L	Н	L	L	L	L	L	L	L	blank
L	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	L	blank
L	Н	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	blank
Н	Н	Н	×	×	×	×				*				*

Note) X : don't care \* : defined by the added BCD code at EL = L

# Logic Diagram







(Output Stage Schematic Diagram)

# MN4512B/MN4512BS

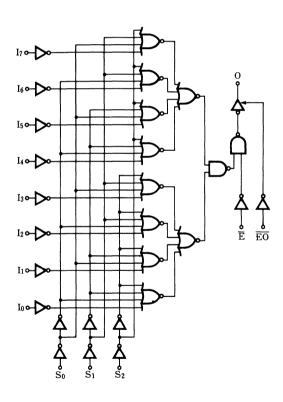
# 8-Input Multiplexers

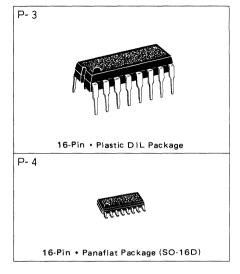
#### Description

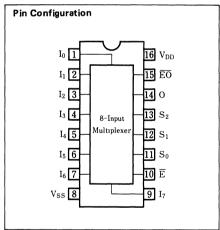
The MN4512B/S are 8-channel data selectors which select data inputs ( $I_0 \sim I_7$ ) by select inputs ( $S_0$ ,  $S_1$ ,  $S_2$ ). A High on the output enable forces the output high impedance (tristate), independent of any other conditions.

A High on the inhibit input  $(\overline{E})$  and a Low on the enable output  $(\overline{EO})$  inhibits the data select, and the output  $(\overline{O})$  becomes Low. The MN4513B/S are equivalent MOTOROLA MC14512B and RCA CD4512B.

#### Logic Diagram







#### Pin Explanation

 $S_0$ ,  $S_1$ ,  $S_2$ : Select input

 $\begin{array}{lll} \overline{EO} & : & Output \ enable \ input \\ \overline{E} & : & Inhibit \ input \\ I_0{\sim}I_7 & : & Multiplexer \ input \\ O & : & Multiplexer \ output \end{array}$ 

# Truth Table

Input													Output
ΕŌ	Ē	S2	Sı	S <sub>0</sub>	I <sub>o</sub>	Ιı	I <sub>2</sub>	$I_3$	I.	I <sub>5</sub>	$I_6$	I,	0
L	Н	×	×	×	×	×	×	×	×	×	×	×	L
L	L	L	L	L	L	×	×	×	×	×	×	×	L
L	L	L	L	L	Н	×	×	×	×	×	×	×	Н
L	L	L	L	Н	×	L	×	×	×	×	×	×	L
L	L	L	L	Н	×	Н	×	×	×	×	×	×	Н
L	L	L	Н	L	×	×	L	×	×	×	×	×	L
L	L	L	Н	L	×	×	Н	×	×	×	×	×	Н
L	L	L	Н	Н	×	×	×	L	×	×	×	×	L
L	L	L	Н	Н	×	×	×	Н	×	×	×	×	Н
L	L	Н	L	L	×	×	×	×	L	×	×	×	L
L	L	Н	L	L	×	×	×	×	Н	×	×	×	Н
L	L	Н	L	Н	×	×	×	×	×	L	×	×	L
L	L	Н	L	H	×	×	×	×	×	Н	×	×	H
L	L	Н	Н	L	×	×	×	×	×	×	L	×	L
L	L	Н	Н	L	×	×	×	×	×	×	Н	×	Н
L	L	Н	Н	Н	×	×	×	×	×	×	×	L	L
L	L	Н	Н	Н	×	×	×	×	×	×	×	Н	Н
Н	×	×	×	×	×	×	×	×	×	×	×	×	Z

Note)

X : don't careZ : high impedance (OFF Mode)

# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	mW
(per package)	Ta=+60~+85°C	$P_D$	Decrease up to 200mW rating at 8mW/°C	mvv
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	<b>−40∼+85</b>	°C
Storage Temperatur	torage Temperature		-65~+150	$^{\circ}$

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V



# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	V <sub>DD</sub>	Sym-		Conditions	Ta=-	-40°C	Ta=	<b>25</b> ℃	Ta=	<b>85</b> ℃	T 7 14
Item	(V)	bol	`	Conditions	min.	max.	min.	max.	min.	max.	Unit
0	5				_	20		20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I}=V_{SS}$ or	$V_{DD}$		40		40	_	300	μA
	15					80		80		600	
	5		$V_I = V_{SS}$ or	17		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I} - V_{\rm SS} $ or $ I_{\rm O}  < 1 \mu A$	V <sub>DD</sub>		0.05		0.05	_	0.05	V
	15		10  < 1 µA		_	0.05		0.05	_	0.05	
	5		¥7¥7	17	4.95		4.95		4.95		
Output Voltage High Level	10	VoH	$V_{\rm I} = V_{\rm SS}$ or	$V_{\mathrm{DD}}$	9.95		9.95	_	9.95	_	V
	15		$ I_0  < 1\mu A$		14.95		14.95	_	14.95	_	
	5			V <sub>0</sub> =0.5V or 4.5V		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V
	15			Vo=1.5V or 13.5V		4		4		4	
* . ** 1.	5			Vo=0.5V or 4.5V	3.5		3.5		3.5	*******	
Input Voltage High Level	10	VIH	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	-	11		11		
_	5		$V_0 = 0.4V$	$V_l = 0 \text{ or } 5V$	0.52		0.44		0.36	-	
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
2011 2011	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6V$	$V_I$ =0 or 5V	0.52		0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_I$ =0 or 10 $V$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	$V_{I}=0 \text{ or } 15V$	3.6		3		2.4		
Output Current High Leve	1 5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_{j} = 0 \text{ or } 1$	5V	_	0.3	_	0.3		1	μA
3-State Leakage Current High Le	vel 15	I <sub>ozh</sub>	$V_0 = V_{DD}$			1.6	_	1.6	_	12	μΑ
Output Pin Leakage Current Low Le	vei 15	$-I_{OZL}$	$V_0 = V_{SS}$			1.6		1.6		12	μΑ

# 

Item	$V_{\mathrm{DD}}\left(\mathbf{V}\right)$	Symbol	min.	typ.	max.	Unit
	5			60	180	
Output Rise Time	10	tTLH		30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	tTHL		30	90	ns
	15			20	60	
Propagation Dalay Time	5			100	300	
Propagation Delay Time In→O (L→H)	10	t <sub>PLH</sub>		40	120	ns
In→O (L→n)	15			30	90	
Description Dolar Time	5			100	300	
Propagation Delay Time	10	tPHL		40	120	ns
$In \rightarrow O (H \rightarrow L)$	15		_	30	90	

# ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$ (continued)

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
December Dalan Time	5			150	450	
Propagation Delay Time	10	t <sub>PLH</sub>	_	60	180	ns
$Sn \rightarrow O (L \rightarrow H)$	15		_	40	120	
Dalan Time	5			140	420	
Propagation Delay Time	10	$\mathbf{t}_{\mathtt{PHL}}$		55	165	ns
Sn→O (H→L)	15			40	120	
Propagation Delay Time	5			55	165	
$\overline{E} \rightarrow O (L \rightarrow H)$	10	t <sub>PLH</sub>		25	75	ns
E→O (L→H)	15			20	60	
Propagation Delay Time	5			60	180	
From E $\rightarrow$ O (H $\rightarrow$ L)	10	t <sub>PHL</sub>		25	75	ns
E→0 (H→L)	15		-	20	60	
High I and Ontrod Dischla Time	5			35	105	
High Level Output Disable Time <del>EO</del> →O (H)	10	$t_{ m PHZ}$		20	60	ns
EO→O (H)	15			15	45	
I am I am I O Di . I I	5		_	35	105	
Low Level Output Disable Time $\overline{EO} \rightarrow O$ (L)	10	$t_{PLZ}$		15	45	ns
EO→O (L)	15			10	30	
High Level Output Enable Time	5			35	105	
EO→O (H)	10	t <sub>PZH</sub>	_	15	45	ns
ЕО→О (П)	15			10	30	
I I 1 O 4 4 E 1 1 - Ti	5		_	35	105	
Low Level Output Enable Time	10	t <sub>PZL</sub>		20	60	ns
$\overline{EO} \rightarrow O (L)$	15			15	45	
Input Capacitance		C <sub>I</sub>			7.5	pF



# MN4514B/MN4514BS

4-Bit Latch / Line Decoders (High)

#### Description

The MN4514B/S are decoders which convert 4-bit input to 16-bit output with the function of latching the input data. Only the selected output becomes "H".

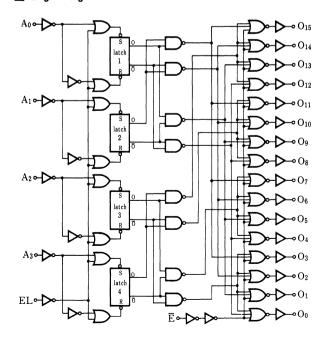
The latch is an R-S type flip-flop and input data is held immediately before the strobe input changes from "H" to "L".

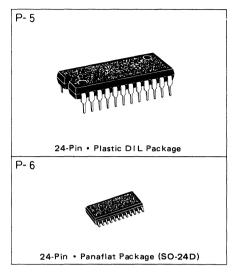
#### Truth Table

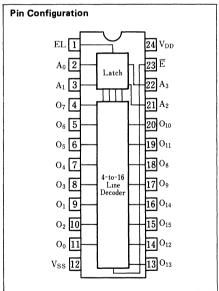
	I	npu	t			Output														
E	A <sub>0</sub>	Aı	A <sub>2</sub>	A <sub>3</sub>	$O_0$	$O_1$	$O_2$	O <sub>3</sub>	04	O <sub>5</sub>	O <sub>6</sub>	07	08	O9	010	011	012	013	014	O <sub>15</sub>
Н	×	×	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	Н	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н	Н	L	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	Н	L	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	L
L	Н	L	Н	L	L	L	L	L	L	Н	L	L	L	L	L	L	L	L	L	L
L	L	Н	Н	L	L	L	L	L	L	L	Н	L	L	L	L	L	L	L	L	L
L	Н	Н	Н	L	L	L	L	L	L	L	L	Н	L	L	L	L	L	L	L	L
L	L	L	L	Н	L	L	L	L	L	L	L	L	Н	L	L	L	L	L	L	L
L	Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н	L	L	L	L	L	L
L	L	Н	L	Н	L	L	L	L	L	L	L	L	L	L	Н	L	L	L	L	L
L	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	L	L	Н	L	L	L	L
L	L	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	Н	L	L	L
L	Н	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	L	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	L
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н

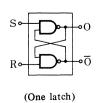
Note) EL = H; X : don't care

#### Logic Diagram









# $\blacksquare$ Maximum Ratings $(Ta=25^{\circ}C)$

Ite	n	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	Λ.
Input Voltage		$V_{I}$	-0.5~V <sub>DD</sub> +0.5*	Λ.
Output Voltage		$V_O$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	Current	± I <sub>1</sub>	max. 10	m.A
Power Dissipation	Ta=-40~+60°C	D	max. 400	111
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (1	per output terminal)	$P_{\mathrm{D}}$	max. 100	шN
Operating Ambient Temperature		Topr	-40~+85	r
Storage Temperatur	e	Tstg	-65~+150	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

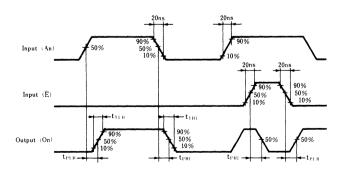
T4 a	$V_{\rm DD}$	Sym-			$T_a = -$	-40℃	Ta=	25℃	Ta=85℃		T I 4
Item	(V)	bol		onditions	mın.	max.	min.	max	mın.	max.	Unit
Ouissant Bauer	5				_	20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	-	40	_	40		300	$\mu$ A
	15					80	_	80		600	
_	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	-	0.05		0.05	_	0.05	V
	15		$ 1_0  < 1\mu A$			0.05	_	0.05		0.05	
0 4 4 17 1	5		V V	NI.	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu$ A	$V_{ m DD}$	9.95		9.95	_	9.95	-	V
	15		$ 1_0  < 1 \mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1 \mu A$	Vo=1V or 9V		3	_	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4	_	4	
T X7. 14	5			Vo=0.5V or 4.5V	3.5		3.5	_	3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7	_	V
	15			Vo=1.5V or 13.5V	11		11	_	11		
	5		$V_0 = 0.4 V$ ,	$V_I$ =0 or 5V	0.52	_	0.44	_	0.36	_	
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I {=} 0 \ or \ 10 V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0$ or $15V$	3.6		3	_	2.4		
	5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5V	0.52		0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I'=0 \text{ or } 10\mathrm{V}$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6		3	_	2.4	-	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5 $V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	SV	_	0.3		0.3	_	1	μA



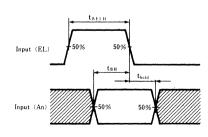
Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	85	255	
Output Rise Time (Fig. 1)	10	t <sub>TLH</sub>		35	105	ns
	15		_	25	75	
	5		_	90	270	
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>	_	35	105	ns
	15		_	25	75	
Propagation Delay Time (Fig. 1)	5		_	270	810	
An, EL-On (L-H)	10	tPLH	_	95	285	ns
An, EL→On (L→H)	15		_	65	195	
D. T. (Fig 1)	5		_	260	780	
Propagation Delay Time (Fig. 1)	10	tPHL	_	95	285	ns
An, $EL \rightarrow On (H \rightarrow L)$	15		_	65	195	
Propagation Delay Time (Fig. 1)	5			200	600	
From E $\rightarrow$ On (L $\rightarrow$ H)	10	$t_{\rm PLH}$		70	210	ns
E→On (L→H)	15		_	50	150	
Propagation Delay Time (Fig. 1)	5			175	525	
E→On (H→L)	10	tPHL		65	195	ns
E→On (H→L)	15			45	135	
(5)	5		_	60	180	
Minimum EL Pulse (Fig. 2) Width	10	twelh	_	20	60	ns
Width	15			15	45	
C. T. (Fig. 2)	5		_	60	180	
Set-up Time (Fig. 2) An→EL	10	tsu	_	20	60	ns
An→EL	15			15	45	
Hold Time (Fig. 2)	5		0	60	_	
	10	thold	0	20	_	ns
An→EL	15		0	15	_	
Input Capacitance		Cı		_	7.5	pF

#### • Dynamic Signal Waveforms

(Fig. 1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}$ ,  $t_{PHL}$ 



(Fig. 2) twell, tsu, thold



Waveforms showing minimum pulse width for EL, set-up and hold times for  $A_{\Pi}$  to EL Set-up and hold times are shown as positive values but may be specified as negative values.

# MN4515B/MN4515BS

4-Bit Latch / Line Decoders (Low)

#### Description

The MN4515B/S are decoders which convert 4-bit input to 16-bit output with the function of latching the input data. Only the selected output becomes "L".

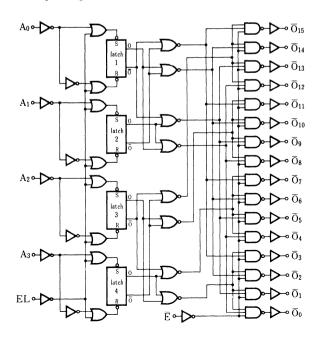
The latch is an R-S type flip-flop and input data is held immediately before the strobe input changes from "H" to "L".

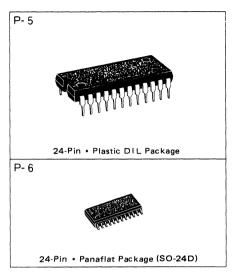
#### Truth Table

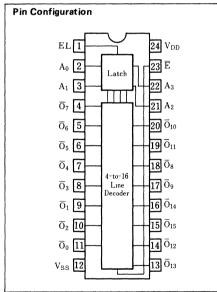
Input					Output															
Е	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	ō	$\bar{O}_1$	$\overline{O}_2$	Ō₃	Ō4	$\overline{O}_5$	$\overline{O}_6$	Ō7	$\bar{O}_8$	Ō9	Ō10	011	Ō12	Ō <sub>13</sub>	Ō <sub>14</sub>	$\overline{O}_{15}$
Н	X	×	×	×	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	.H
L	Н	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	Н	L	L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Η	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	Н	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

Note) EL = H; X : don't care

## Logic Diagram











# ■ Maximum Ratings (Ta=25°C)

Ite	em	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		Vı	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{\rm I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	$^{\circ}$
Storage Temperatu	re	Tstg	-65~+150	$^{\circ}$

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

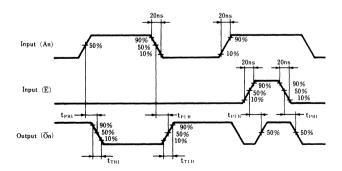
T4	$V_{\mathrm{DD}}$	Sym-	Conditions		Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	(	onditions	min.	max.	min.	max.	min.	max.	Unit
	5				_	20		20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	40	-	40	_	300	μA
	15				80		80	_	600		
	5		$V_I = V_{SS}$ or	V		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_{\rm I}-V_{\rm SS} $ or $ I_{\rm O} <1\mu{\rm A}$	<b>v</b> DD	_	0.05		0.05	_	0.05	V
	15		$ 1_0  < 1\mu A$		-	0.05		0.05	_	0.05	
0	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95	_	4.95		1.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	9.95		9.95		9.95	_	V
	15		101/101		14.95		14.95		14.95		
* ***	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	_	1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V		3	-	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4		4		4	
Input Voltage	5		$ I_{\rm O}  < 1\mu A$	$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
High Level	10	$V_{IH}$		V <sub>0</sub> =1V or 9V	7		7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11	_	11		
0 6	5		$V_0 = 0.4 V$	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Out and Out of	5		$V_0 = 4.6 V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I{=}0\ or\ 10V$	1.3		1.1		0.9	-	mA
	15		$V_0 = 13.5 V$	, V <sub>1</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_i = 0 \text{ or } 15$	5V		0.3		0.3		1	μA

# ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

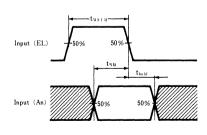
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		_	85	255		
Output Rise Time (Fig. 1)	10	t <sub>TLH</sub>	_	35	105	ns	
_	15			25	75		
	5		_	90	270		
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>		35	105	ns	
	15		_	25	75		
D (Fig. 1)	5		_	270	810		
Propagation Delay Time (Fig. 1)	10	t <sub>PLH</sub>	_	95	285	ns	
An, $EL \rightarrow \overline{O}n \ (L \rightarrow H)$	15		_	65	195		
Propagation Delay Time (Fig. 1)	5		_	260	780		
Propagation Delay Time $\langle -13, -1 \rangle$ An, $EL \rightarrow \overline{O}n \ (H \rightarrow L)$	10	t <sub>PHL</sub>		95	285	ns	
An, EL→On (H→L)	15		_	65	195		
Propagation Delay Time (Fig. 1)	5			200	600		
$E \rightarrow \overline{O}n  (L \rightarrow H)$	10	t <sub>PLH</sub>	_	70	210	ns	
E→On (L→H)	15			50	150		
Propagation Delay Time (Fig. 1)	5		_	175	525		
$\overline{E} \rightarrow \overline{O}n  (H \rightarrow L)$	10	t <sub>PHL</sub>	_	65	195	ns	
E→On (H→L)	15	}	_	45	135	ı	
(Fig. 2)	5		_	60	180		
Minimum EL Pulse (Fig. 2) Width	10	twelh	_	20	60	ns	
	15			15	45		
Set-up Time (Fig. 2)	5		_	60	180		
An→EL	10	tsu	_	20	60	ns	
An→EL	15			15	45		
Hold Time (Fig. 2)	5		0	60			
Hold Time (1.2.2) An→EL	10	thold	0	20		ns	
All→EL	15		0	15			
Input Capacitance		$C_{I}$	_		7.5	pF	

## • Dynamic Signal Waveforms

(Fig. 1)  $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PLH}$ ,  $t_{PHL}$ 



(Fig. 2)  $t_{WELH}$ ,  $t_{su}$ ,  $t_{hold}$ 



Waveforms showing minimum pulse width for EL, set-up and hold times for  $A_{\text{n}}$  to EL; set-up and hold times are shown as positive values but may be specified as negative values.

# MN4516B/MN4516BS

# 4-Bit Binary Up/Down Counters

#### Description

The MN4516B/S are 4-bit synchronous up/down counters. An appropriate value of the counter is presettable by setting data inputs ( $P_0 \sim P_3$ ) while the reset input is Low and the load input High.

The counter advances on the positive going edge of the clock input when the load and the counter inputs are low.

A High on the reset input resets all the outputs  $(O_0 \sim O_3)$  Low. The  $UP/\overline{DN}$  input determines whether the counter functions up or down (H = UP, L = DOWN).

The MN4516B/S are equivalent to MOTOROLA MC14516B and RCA CD4516B.

#### Truth Table

MR	PL	UP/DN	ĈĒ	CP	Mode
L	Н	×	×	×	parallel load
L	L	×	Н	×	no change
L	L	L	L		count down
L	L	Н	L		count up
Н	×	×	×	×	liset

#### Pin Explanation

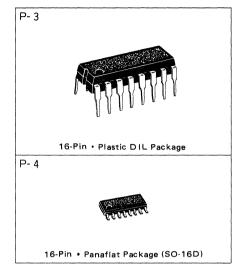
CP : Clock input

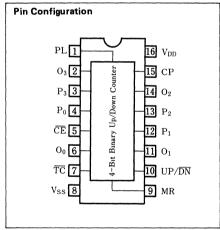
UP/DN: Up, Down designate input

PL : Counter load input

 $\overline{CE}$ : Counter enable input

 $\begin{array}{ccc} MR & \vdots & Reset \ input \\ P_0 \sim P_3 : & Data \ input \\ O_0 \sim O_3 : & Counter \ output \\ \overline{TC} & \vdots & Carry \ output \end{array}$ 





# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	$-0.5 \sim +18$	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	11/
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	e	Tstg	-65~+150	C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{\rm SS}\!=\!0V)$

T4	$V_{\mathrm{DD}}$	Sym-		34141	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
Onima P	5				_	20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	VDD		0.05	_	0.05	_	0.05	V
	15		10  \ 1 \mu A			0.05		0.05		0.05	
Ontant Walter	5		$V_i = V_{SS}$ or	V	4.95		4.95	_	4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	<b>v</b> DD	9.95		9.95		9.95		V
	15		10  \ 1μΛ		14.95		14.95	-	14.95	-	
Y	5		$ I_{\rm O}  < 1\mu{\rm A}$	Vo=0.5V or 4.5V		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL		Vo=1V or 9V		3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Input Voltage	5		$ I_{\rm O}  < 1\mu A$	Vo=0.5V or 4.5V	3.5		3.5		3.5		
High Level	10	$V_{IH}$		Vo=1V or 9V	7		7	_	7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0=0.4V$	$V_I = 0$ or $5V$	0.52		0.44	-	0.36	-	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I {=} 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
0 0	5	}	$V_0=4.6V$	$V_I = 0$ or $5V$	0.52	_	0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
-	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I = 0 \text{ or } 5V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_{\rm I} = 0$ or 15	5V		0.3		0.3		1	μA



**Switching Characteristics** ( $Ta = 25^{\circ}C$ ,  $V_{SS} = 0V$ ,  $C_L = 50pF$ )

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		_	60	180		
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns	
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10 t <sub>THL</sub>		_	30	90	ns	
	15			20	60		
D	5		_	145	435		
Propagation Delay Time	10	t <sub>PHL</sub>	_	60	180	ns	
$CP \rightarrow On (H \rightarrow L)$	15		_	45	135		
D	5		_	155	465		
Propagation Delay Time	10	t <sub>PLH</sub>	_	65	195	ns	
$CP \rightarrow On (L \rightarrow H)$	15	-12	_	45	135		
	5		<del>                                     </del>	260	780		
Propagation Delay Time	10	t <sub>PHL</sub>		105	315	ns	
$CP \rightarrow \overline{TC} (H \rightarrow L)$	15	VERL	_	75	225		
	5			180	540		
Propagation Delay Time	10	t <sub>PLH</sub>		75	225	ns	
$CP \rightarrow \overline{TC} (L \rightarrow H)$	15	•РЕН		55	165	113	
	5			125	375		
Propagation Delay Time	10			55	165	20	
$PL \rightarrow On (H \rightarrow L)$		t <sub>PHL</sub>	_			ns	
	15		<del></del>	40	120		
Propagation Delay Time	5		-	170	510		
$PL \rightarrow On (L \rightarrow H)$	10	t <sub>PLH</sub>	_	70	210	ns	
	15			50	150		
Propagation Delay Time	5		_	250	750		
$PL \rightarrow \overline{TC} (H \rightarrow L)$	10	t <sub>PHL</sub>	_	110	330	ns	
	15			80	240		
Propagation Delay Time	5		_	250	750		
$PL \rightarrow \overline{TC} (L \rightarrow H)$	10	$\mathbf{t}_{\mathtt{PLH}}$	_	110	330	ns	
	15		_	80	240		
Propagation Delay Time	5		_	165	495		
$\overline{CE} \rightarrow \overline{TC} (H \rightarrow L)$	10	t <sub>PHL</sub>	_	65	195	ns	
	15			50	150		
Propagation Delay Time	5		_	145	435		
$\overline{CE} \rightarrow \overline{TC} (L \rightarrow H)$	10	t <sub>PLH</sub>	_	60	180	ns	
CE TO (E-II)	15		_	45	135		
Propagation Delay Time	5		_	205	615		
MR $\rightarrow$ On, $\overline{TC}$ (H $\rightarrow$ L)	10	t <sub>PHL</sub>	_	65	195	ns	
MR-On, IC (H-L)	15			45	135		
Propagation Delay Time	5		_	225	675		
	10	t <sub>PLH</sub>	_	75	225	ns	
$MR \rightarrow \overline{TC} (L \rightarrow H)$	15		_	50	150		
4-14	5			45	135		
Minimum Clock Pulse (Fig. 1)	10	twcpl	_	20	60	ns	
Width	15	- HOFE	_	15	45		

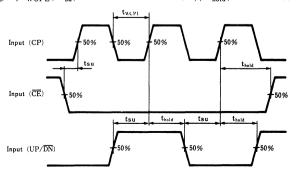
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# ■ Switching Characteristics $(Ta=25\%, V_{SS}=0V, C_L=50pF)$ (countinued)

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit	
(5)	5			55	165		
Minimum PL Pulse (Fig. 2) Width (H)	10	twPLH	_	25	75	ns	
width (H)	15		_	15	45		
(5)	5		_	60	180		
Minimum Reset Pulse (Fig. 2) Width (H)	10	twmRH	_	25	75	ns	
widin (n)	15		-	20	60		
	5	t <sub>RMR</sub>	_	65	195		
Reset Recovery Time (Fig. 2)	10			20	60	ns	
	15		_	15	45		
	5		_	75	225		
PL Recovery Time (Fig. 2)	10	t <sub>RPL</sub>	_	25	75	ns	
	15		_	15	45		
Set-up Time (Fig. 2)	5		_	50	150		
Pn→PL	10	tsu	_	25	75	ns	
Pn→PL	15		-	20	60		
Set-up Time (Fig. 1)	5		_	125	375		
UP/DN→CP	10	tsu	_	50	150	ns	
UP/DN→CP	15		_	35	105		
Set-up Time (Fig. 1)	5		_	60	180		
<del>CE</del> →CP	10	tsu	_	20	60	ns	
CE→CF	15		_	10	30		
Hold Time (Fig. 2)	5			-40	10		
Pn→PL	10	thold	_	-20	5	ns	
rn→rL	15		_	-20	0		
Hold Time (Fig, 1)	5			-90	35		
UP/DN→CP	10	thold	_	-35	15	ns	
UP/DN→CP	15		_	-25	15		
Hold Time (Fig. 1)	5		_	-40	20		
Hold Time (1.45. 1) <del>CE</del> →CP	10	thold	_	-15	5	ns	
CE→CP	15		_	-10	5		
	5		5	10	_		
Maximum Clock Frequency	10	fmax	12	24	_	MHz	
	15		17	34	-		
Input Capacitance		Cı	_	_	7.5	pF	

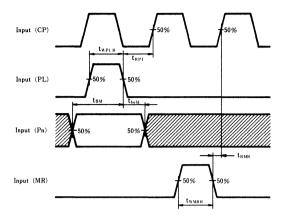
# • Dynamic Signal Waveforms

(Fig. 1)  $t_{WCPL}$ ,  $t_{su}(UP/\overline{DN} \rightarrow CP \cdot \overline{CE} \rightarrow CP)$ ,  $t_{hold}(UP/\overline{DN} \rightarrow CP \cdot \overline{CE} \rightarrow CP)$ 



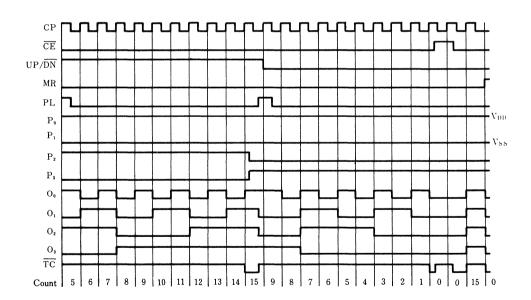
Waveforms showing minimum pulse width for CP, set-up and hold times for  $\overline{\text{CE}}$  to CP and UP/  $\overline{\text{DN}}$  to CP

(Fig. 2)  $t_{WPLH}$ ,  $t_{RPL}$ ,  $t_{RMR}$ ,  $t_{WMRH}$ ,  $t_{SU}(Pn{\rightarrow}PL)$ ,  $t_{hold}(Pn{\rightarrow}PL)$ 



Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR, and set-up and hold times for  $P_\Pi$  to PL

# Timing Diagram



# **New Product Indormation**

Type No.	Function	Pins
MN4014B/S	8-Stage Static Shift Register	16
MN4031B/S	64-Stage Static Shift Register	16
MN4041B/S	Quad True Complement Buffer	14
MN4047B/S	Monostable Astable Multivibrator	14
MN4060B/S	14-Stage Ripple-Carry Binary Counter/Divider and Oscillator	16
MN4077B/S	Quad Exclusive-NOR Gate	14
MN4104B/S	Quad Low Voltage to High Voltage Translator with 3/5	16
MN4505B/S	64×1-Bit Static RAM	14
MN4521B/S	24-Stage Frequency Divider	16
MN4522B/S	Programmable BCD Divide-by-N Counter	16
MN4527B/S	BCD Rate Multiplier	16
MN4532B/S	8-Bit Priority Encoder	16
MN4555B/S	Dual Binary to 1-of-4 Decoder/Demultiplexer	16
MN4557B/S	1-of-64-Bit Variable Length Shift Register	16
MN4720B/S	256-Bit, 1-Bit-per-Word RAM	16
MN4731B/S	Quad 64-Bit Static Shift Register	14
MN40162B/S	Decade Counter with Synchronous Clear	16
MN40163B/S	4-Bit Binary Counter with Synchronous Clear	16
MN40192B/S	4-Bit Up/Down Decade Counter	16
MN40193B/S	4-Bit Up/Down Binary Counter	16
MN40194B/S	4-Bit Bidirectional Universal Shift Register	16
MN40195B/S	4-Bit Universal Shift Register	16

Note) Under development

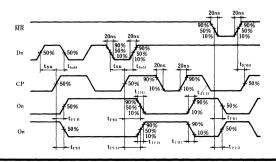
# New Product Information



■ Switching Characteristics  $(Ta=25^{\circ}C, V_{SS}=0V, C_{L}=50pF)$ 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	80	240	
CP→On, On (H→L)	10	t <sub>PHL</sub>	_	35	105	ns
CP→On, On (H→L)	15		_	25	75	
Propagation Dolay Time	5		_	70	210	
Propagation Delay Time CP→On, Ōn (L→H)	10	t <sub>PLH</sub>	_	30	90	ns
	15		_	25	75	
D	5		_	75	225	
Propagation Delay Time	10	$t_{ ext{PHL}}$	_	30	90	ns
$\overline{MR} \rightarrow On \ (H \rightarrow L)$	15		_	25	75	
Propagation Delay Time $\overline{MR} \rightarrow \overline{O}n \ (L \rightarrow H)$	5		_	70	210	
	10	tplh	_	30	90	ns
	15		_	25	75	
C Ti	5		_	30	90	
Set-up Time Dn→CP	10	tsu	_	10	30	ns
Dn→CP	15		_	5	15	
Hold Time	5		_	- 5	30	
Dn→CP	10	$t_{hold}$	_	0	15	ns
Dn-Cr	15		_	0	15	
	5			45	135	
Minimum Clock Pulse Width	10	twcpl	_	15	45	ns
	15			10	30	
	5		_	40	120	
Minimum Reset Pulse Width	10	twmrL	_	15	45	ns
	15			10	30	
	5		_	-30	0	
Reset Recovery Time	10	t <sub>RMR</sub>	_	-20	0	ns
	15			-15	0	
	5		5	11		
Maximum Clock Frequency	10	fmax	15	30		MHz
	15		20	45	_	
Input Capacitance		Cı	_	_	7.5	pF

### • Dynamic Signal Waveforms



### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		$V_{O}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	147
(per package)	Ta=+60~+85℃	$\mathbf{P}_{\mathtt{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (1	per output terminal)	$P_D$	max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	e	Tstg	-65~+150	$^{\circ}$

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{\rm SS}{=}0V)$

_	$V_{ m DD}$	Sym-		••••	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
Item	(V)	bol	C	onditions	min.	max.	min.	max.	min.	max.	Unit
Ouiescent Power	5				_	20	_	20		150	
Supply Current	10	$I_{\mathrm{DD}}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
our page 1	15					80		80		600	
	5		V-V	$V_I = V_{SS}$ or $V_{DD}$		0.05		0.05		0.05	
Output Voltage Low Level	10	Vol		VDD		0.05	_	0.05		0.05	V
Dow Level	15		$ 10  \leq 1 \mu A$	$I_{\mathrm{O}}  < 1\mu\mathrm{A}$		0.05		0.05		0.05	
0	5		V-V	V	4.95	_	4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	$\mathbf{v}_{\mathrm{DD}}$	9.95		9.95	*****	9.95		V
	15		$ 1_0  < 1\mu$ A		14.95		14.95		14.95		
	5			Vo=0.5V or 4.5V	_	1.5	-	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3		3	V
20 21	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
x , x7 1,	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	V <sub>IH</sub>	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7	_	7		7	_	V
	15			Vo=1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4 V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
20.1. 20.01	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \text{V}$	3.6		3		2.4		
	5		$V_0 = 4.6V$ ,	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5 V$ ,	$V_i = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9		mA
11.g. 22-1-1	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 19$	5V		0.3		0.3	_	1	μΑ



# MN40175B/MN40175BS

Quad D-Type Flip-Flops

### Description

The MN40175B/S have quad D-type flip-flop which have common CP and  $\overline{MR}$  pins

 $\boldsymbol{D}_n$  input is transferred to  $\boldsymbol{O}_n$  output on the positive going edge of clock input.

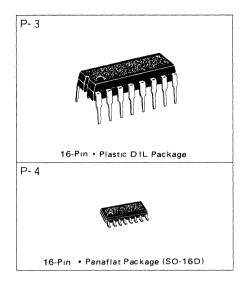
When the  $\overline{MR}$  input becomes "L" level, the quad flip-flop can be reset at the same time.

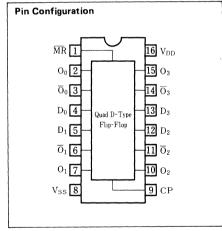
These are equivalent to MOTOROLA MC14715B.

### Truth Table

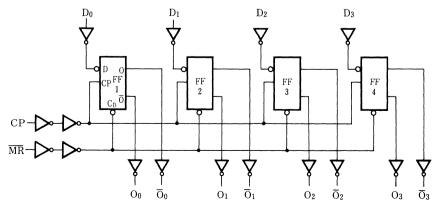
	Input		Output			
CP	D	MR	0	ō		
	Н	Н	Н	L		
	L	Н	L	Н		
7	×	Н	no change	no change		
×	×	L	L	Н		

Note) X: don't care





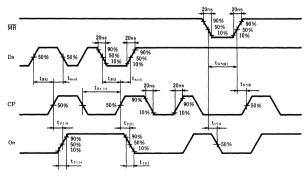
### Logic Diagram



### ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	į
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
	5		_	75	225	
Propagation Delay Time	10	tphL		30	90	ns
CP→On (H→L)	15		_	20	60	
	5			75	225	
Propagation Delay Time	10	t <sub>PLH</sub>	_	30	90	ns
$CP \rightarrow On (L \rightarrow H)$	15		_	20	60	
December 1	5		_	85	255	
Propagation Delay Time	10	t <sub>PHL</sub>		35	105	ns
$\overline{MR} \rightarrow On (H \rightarrow L)$	15	1.02	_	25	75	
	5		_	10	30	
Set-up Time Dn→CP	10	tsu	_	5	15	ns
	15			5	15	
	5			0	20	
Hold Time	10	$t_{hold}$		0	10	ns
Dn→CP	15	-nora		0	10	
	5			35	100	<del> </del>
Minimum Clock Pulse Width	10	twcpl	_	15	45	ns
	15	JWCFE	_	10	30	
	5			35	100	<u> </u>
Minimum MR Pulse Width	10	twmrL		15	45	ns
	15	WMR1.	_	10	30	
	5		_	25	75	
Reset Recovery Time	10	t <sub>RMR</sub>		10	30	ns
	15	KMK	_	5	15	5
	5	+	5	11		+
Maximum Clock Frequency	10	fmax	15	30		MHz
Maximum Clock Prequency	15	ımax	20	45	_	WIIIZ
Input Capacitance	10	Cı	20	40	7.5	pF

### • Dynamic Signal Waveforms





### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	$-0.5 \sim +18$	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		$V_{\rm O}$	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output	t Current	$\pm I_{I}$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	mW	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C		
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	<b>−40~+85</b>	°C	
Storage Temperatur	re	Tstg	-65~+150	°C	

<sup>\*</sup>V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS} {=} 0V)$

Item	V.DD	Sym-		Conditions	Ta=-	-40°C	Ta=	25℃	Ta=	85℃	
	(V)	bol	`	Conditions	min.	max.	min.	max.	min.	max.	Unit
Ouissess Passes	5					20		20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$		40	—	40	_	300	μA
	15					80	-	80	_	600	
0	5		V-V	V	_	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ I_{\rm O}  < 1\mu A$	$V_{\rm I} = V_{\rm SS} \text{ or } V_{\rm DD}$		0.05		0.05		0.05	V
	15		10) < 1µA			0.05	_	0.05	_	0.05	
0-1-17	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95	_	4.95		4.95	_	
Output Voltage High Level	10	VoH	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	$\mathbf{v}_{\mathrm{DD}}$	9.95	_	9.95		9.95	_	V
	15		10  < 1μA		14.95		14.95		14.95	_	
	5			Vo=0.5V or 4.5V	_	1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3		3	_	3	V
-	15			Vo=1.5V or 13.5V	_	4	_	4	-	4	
Innut Valtage	5			Vo=0.5V or 4.5V	3.5	_	3.5		3.5	_	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7	_	7	_	7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11		11	_	
0.1	5		$V_0 = 0.4 V$	$V_I$ =0 or 5 $V$	0.52		0.44		0.36	_	
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0$ or $15V$	3.6		3	_	2.4	_	
0 0	5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5V	0.52		0.44	_	0.36	_	
Output Current High Level	10	$-I_{\text{OH}}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1	_	0.9		mA
	15		$V_0 = 13.5 V_1$	, $V_I$ =0 or 15 $V$	3.6	_	3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7		1.4	_	1.1	_	mA
Input Leakage Current	15	$\pmI_I$	$V_I = 0$ or 15	V	_	0.3	_	0.3	_	1	μA

# MN40174B/MN40174BS

Hex D-Type Flip-Flops

### Description

The MN40174B/S have hex D-type flip-flops with common CP and MR pins.

 $D_n$  input is transferred to  $O_n$  output on the positive going edge of clock input.

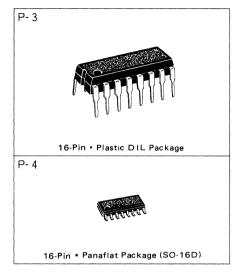
When the MR input level becomes "L", hex flip-flop can be reset at the same time.

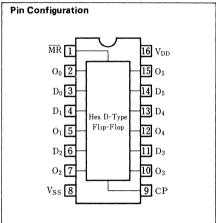
The MN40174B/S are equivalent to MOTOROLA MC14174B and RCA CD40174B.

### Truth Table

	Input		Output
CP	D	MR	0
	Н	Н	Н
	L	Н	L
	×	Н	no change
×	×	L	L

Note) X : don't care





### Logic Diagram

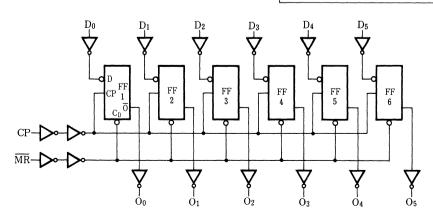
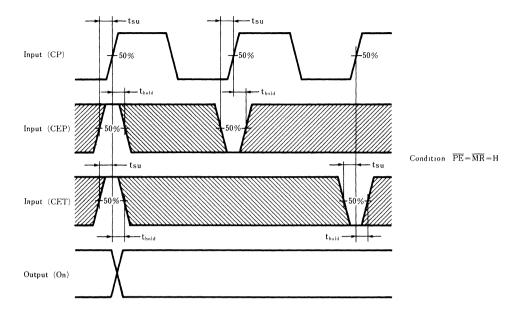


Fig. 4 Dynamic Signal Waveforms (CEP, CET → CP)



### Timing Diagram

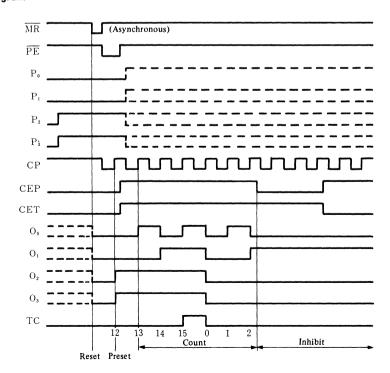


Fig. 1 Dynamic Signal Waveforms (CP, MR)

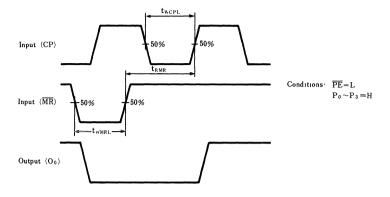


Fig. 2 Dynamic Signal Waveforms  $(P_n \rightarrow CP)$ 

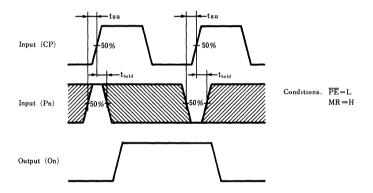
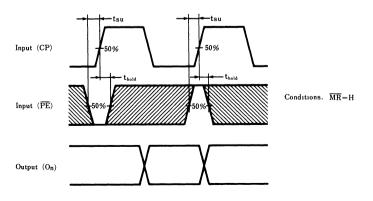


Fig. 3 Dynamic Signal Waveforms (PE → CP)





 $\blacksquare$  Switching Characteristics  $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_L\!=\!50pF)$  (continued)

Switching Characteristics	(1a-25C,	VSS-0 V, C	L-30pr) (	oontinued j		
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	115	345	
CP→On (L→H)	10	$t_{PLH}$		45	135	ns
CP→On (L→H)	15		_	35	105	i
Propagation Delay Time	5			110	330	
* *	10	$t_{ m PHL}$		45	135	ns
CP→On (H→L)	15			30	90	
Propagation Delay Time	5			140	420	
	10	t <sub>PLH</sub>	_	55	165	ns
$CP \rightarrow TC \ (L \rightarrow H)$	15		_	40	120	
Propagation Delay Time	5		_	130	390	
	10	tPHL	_	55	165	ns
$CP \rightarrow TC \ (H \rightarrow L)$	15		-	40	120	
Drama sation Dalay Time	5		_	90	270	
Propagation Delay Time	10	t <sub>PLH</sub>	_	35	105	ns
$CET \rightarrow TC \ (L \rightarrow H)$	15			25	75	1
Dramagation Dales- Time-	5		_	105	315	
Propagation Delay Time	10	t <sub>PHL</sub>	_	50	150	ns
$CET \rightarrow TC \ (H \rightarrow L)$	15	1	_	35	105	
	5		_	120	360	
Propagation Delay Time	10	t <sub>PHL</sub>	_	50	150	ns
$\overline{MR} \rightarrow On \ (H \rightarrow L)$	15	- THE	_	35	105	
	5			145	435	
Propagation Delay Time	10	t <sub>PHL</sub>		60	180	ns
$\overline{MR} \rightarrow TC \ (H \rightarrow L)$	15	- FRL		45	135	
	5			50	150	
Minimum Clock Pulse (Fig. 1)	10	$t_{\text{WCPL}}$		20	60	ns
Width	15	OWCFL	_	15	45	
	5	-	_	50	150	
Minimum Reset Pulse (Fig. 1)	10	twmrl	_	20	60	ns
Width	15	WMRL		15	45	113
(nt. 4)	5	<del> </del>		0	50	
Reset Recovery Time (Fig. 1)	10	t <sub>RMR</sub>	_	0	30	ns
$\overline{MR}$	15	- KMR	_	0	20	113
(Fig. 2)	5		_	55	165	
Set-up Time (Fig. 2)	10	tsu		20	60	ns
Pn→CP	15	Lou	_	15	45	113
(Fig. 2)	5			60	180	<del> </del>
Set-up Time <sup>(Fig. 3)</sup>	10	ton	_	20	60	ns
PE→CP	15	tsu	_	10	30	ns
	5			<del></del>		
Set-up Time (Fig. 4)	1	4		130	390	
CEP, CET→CP	10	tsu		50	150	ns
	15		-	35	105	
Maximum Clock (Fig. 1)	5	,	5	10	_	3.677
Frequency	10	fmax	12	25		MHz
Immut Comocitono	15	<del> </del>	17	35		
Input Capacitance		C <sub>I</sub>	_	_	7.5	pF

### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		$V_{\rm I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissiption (p	er output terminal)	$P_{D}$	max. 100	mW
Operating Ambient	Temperature	Topr	-40~+85	°C
Storage Temperatur	e	Tstg	$-65 \sim +150$	$^{\circ}$

<sup>\*</sup>V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

7.	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	85℃	Unit
Item	(V)	bol		conditions	min.	max.	min.	max.	min.	max.	Unit
0 :	5				_	20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{\mathrm{DD}}$		40	_	40		300	μA
5 mp p n s	15					80	_	80		600	
	5		XI XI	3.7		0.05		0.05		0.05	
Output Voltage Low Level	10	$V_{OL}$		$V_I = V_{SS}$ or $V_{DD}$		0.05	_	0.05		0.05	V
Low Level	15		$ I_{\rm O}  < 1\mu A$			0.05	_	0.05	-	0.05	
	5		37 37	X 7	4.95		4.95		4.95		
Output Voltage High Level	10	Voh	$V_I = V_{SS}$ or	$V_{ m DD}$	9.95		9.95	**********	9.95	_	V
	15		$ I_{\rm O}  < 1\mu{\rm A}$	$ 10  < 1\mu$ A			14.95		14.95	-	
	5			Vo=0.5V or 4.5V		1.5		1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1 \mu A$	Vo=1V or 9V		3		3		3	V
	15			Vo=1.5V or 13.5V		4		4		4	
7 . 37 1.	5			Vo=0.5V or 4.5V	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			Vo=1.5V or 13.5V	11		11	_	11		
	5		$V_0 = 0.4 V$ ,	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_I{=}0\ or\ 10\mathrm{V}$	1.3		1.1		0.9		mA
2011 20101	15		$V_0 = 1.5 V$ ,	$V_I {=} 0 \text{ or } 15 \text{V}$	3.6		3	_	2.4		
	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I{=}0\ or\ 10V$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	$V_{I} = 0 \text{ or } 15V$	3.6	_	3		2.4	_	
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	$V_i = 0$ or $5V$	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_1 = 0 \text{ or } 15$	5V		0.3	_	0.3	_	1	μА

### 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit	
	5			60	180	ns	
Output Rise Time	10	t <sub>TLH</sub>	******	30	90		
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>		30	90	ns	
	15		_	20	60		



# MN40161B/MN40161BS

### 4-Bit Binary Counters

### Description

The MN40161B/S are synchronous programmable 4-bit binary counters.

The reset functions asynchronously, causing all flip-flop outputs to reset.

The counter advances on the positive going edge of the clock input when both CEP and CET inputs are High and the PE input is also High.

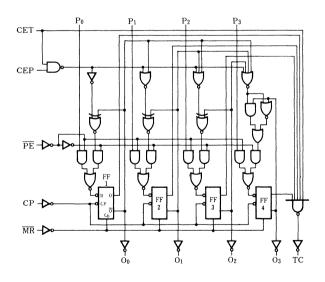
The MN40161B/S are equivalent to MOTOROLA MC14161B and RCA CD40161B.

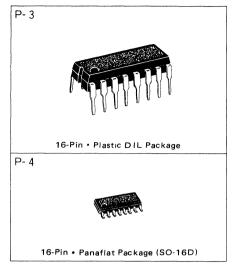
### Truth Table

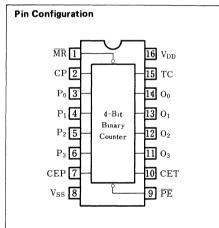
	In	Nr. 4-					
$\overline{MR}$	$\overline{\text{PE}}$	CEP	CET	Mode			
Н	L	×	×	parallel load			
Н	Н	L	×				
Н	Н	×	L	no change			
Н	Н	Н	Н	counter advance			
L	×	×	×	reset (O <sub>0</sub> ~O <sub>3</sub> =L)			

Note) X: don't care

### Logic Diagram







### Pin Explanation

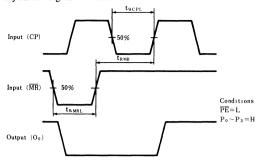
 $\overline{PE}$ : Parallel enable input  $P_0 \sim P_3$ : Parallel data input

CEP : Count enable parallel input
CET : Count enable triple input
CP : Clock input ( \_\_\_\_\_)

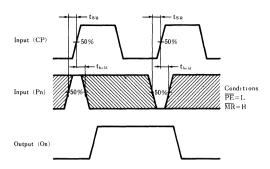
MR : Master reset input

 $O_0 \sim O_3$ : Parallel output TC: Carry output

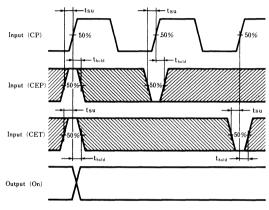
### • Dynamic Signal Waveforms



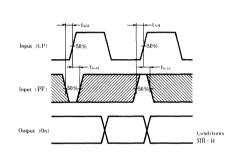
Waveforms showing minimum CP and  $\overline{MR}$  pulse widths and  $\overline{MR}$  to CP recovery time



Waveforms showing set-up times and hold times for  $\boldsymbol{P}_{\boldsymbol{n}}$  inputs

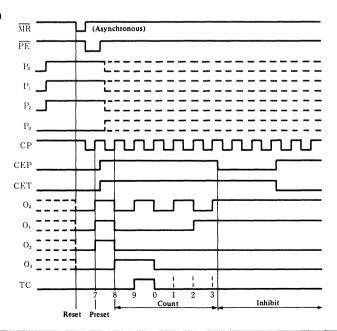


Waveforms showing set-up times and hold times for CEP and CET inputs  $% \left( 1\right) =\left( 1\right) \left( 1\right$ 



Waveforms showing set-up times and hold times for  $\overline{\mbox{PE}}$  inputs.

### Timing Diagram





Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	90	270	
	10	$t_{\rm PLH}$	_	35	105	ns
$CET \rightarrow TC \ (L \rightarrow H)$	15			25	75	1
Propagation Delay Time	5			105	315	
	10	t <sub>PHL</sub>		50	150	ns
$CET \rightarrow TC \ (H \rightarrow L)$	15		_	35	105	
Propagation Delay Time	5		_	120	360	
	10	t <sub>PHL</sub>	_	50	150	ns
$\overline{MR} \rightarrow On \ (H \rightarrow L)$	15		-	35	105	
Propagation Delay Time	5		_	145	435	
	10	t <sub>PHL</sub>		60	180	ns
$\overline{MR} \rightarrow TC \ (H \rightarrow L)$	15		_	45	135	
	5		_	50	150	
Minimum Clock Pulse Width	10	twcpl		20	60	ns
	15		_	15	45	
	5			50	150	
Minimum Reset Pulse Width	10	twmrl	_	20	60	ns
	15		_	15	45	
	5		_	0	50	
Reset Recovery Time	10	$t_{RMR}$	_	0	30	ns
	15		_	0	20	
C.4 Ti	5		_	55	165	
Set-up Time	10	tsu		20	60	ns
Pn→CP	15			15	45	
Sat year Times	5			60	180	
Set-up Time	10	tsu		20	60	ns
<del>PE</del> →CP	15			10	30	
Set-up Time	5			130	390	
*	10	tsu	_	50	150	ns
CEP, CET→CP	15			35	105	
Hold Time	5		_	-35	30	
	10	thold	_	-10	15	ns
Pn→CP	15			-10	10	
Hold Time	5		_	-45	20	
PE→CP	10	thold	_	-15	10	ns
re→Ur	15		_	-10	10	
Hold Time	5		_	-105	35	
	10	thold	_	- 35	25	ns
CEP, CET→CP	15		_	- 25	15	
	5		5	10	_	
Minimum Clock Frequency	10	fmax	12	25	_	MHz
	15		17	35	_	
Input Capacitance		Cı	_	_	7.5	pF

270

# $\blacksquare$ DC Characteristics $(V_{SS}{=}0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Ta=25℃		Ta=85℃		Unit
	(·V )	bol	,	Conditions	min.	max.	min.	max.	min.	max.	Unit
Oviganous Paren	5				-	20		20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS}$ or	$V_{DD}$		40		40		300	μA
	15					80		80		600	
	5		V-V	$V_{\rm I} = V_{\rm SS}$ or $V_{\rm DD}$		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1 \mu A$			0.05		0.05		0.05	V
20 20 . 0.	15		$ 1_0  < 1\mu A$		_	0.05		0.05	_	0.05	
_	5		17 17	T.7	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS} \text{ or } V_{\rm DD}$ $ I_{\rm O}  < 1 \mu\text{A}$		9.95		9.95		9.95		V
	15		$ 1_0  < 1 \mu A$	<sup>4</sup> A			14.95	_	14.95		
	5			Vo=0.5V or 4.5V		1.5	-	1.5		1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3		3	V
20.01	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
T 17.14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			Vo=1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4 V$ ,	V <sub>i</sub> =0 or 5V	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6	_	3	_	2.4		
	5		$V_0 = 4.6V$ ,	V <sub>I</sub> =0 or 5V	0.52	_	0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I$ =0 or 10 $V$	1.3	_	1.1		0.9		mA
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6		3		2.4		
Output Current High Level	5	— I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>i</sub> =0 or 15	SV		0.3		0.3		1	μA

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_L\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left( \mathrm{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
Output Fall Time	5			60	180	
	10	t <sub>THL</sub>		30	90	ns
	15		_	20	60	
Propagation Delay Time CP→On (L→H)	5			115	345	
	10	$t_{\mathtt{PLH}}$	-	45	135	ns
	15			35	105	
Duamanation Dalay Time	5			110	330	
Propagation Delay Time CP→On (H→L)	10	tPHL		45	135	ns
CP→On (H→L)	15		_	30	90	
December 10 -1 Time	5		_	140	420	
Propagation Delay Time	10	$t_{\mathrm{PLH}}$	_	55	165	ns
$CP \rightarrow TC \ (L \rightarrow H)$	15		_	40	120	
Propagation Delay Time	5			130	390	
	10	$t_{ m PHL}$		55	165	ns
$CP \rightarrow TC (H \rightarrow L)$	15			35	105	

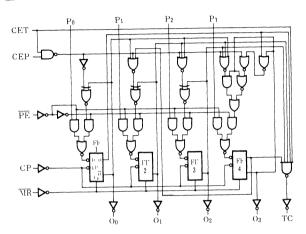
# MN40160B/MN40160BS

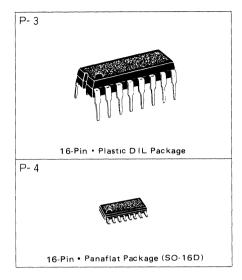
### 4-Bit Decade Counters

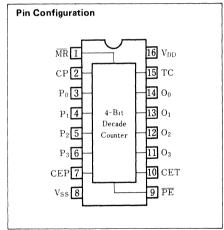
### Description

The MN40160B/S are 4-bit decade counters which have asynchronous clear input.

### Logic Diagram







### Maximum Ratings $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		$\pm I_i$	max. 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	W	
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (per output terminal)		$P_{\mathrm{D}}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

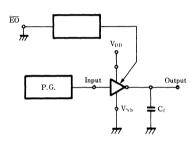
<sup>\*</sup>  $V_{DD}$  + 0 5V should be under 18V

### ■ Switching Characteristics $(Ta=25^{\circ}C, V_{SS}=0V, C_{L}=50pF)$ (continued)

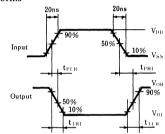
Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
Low Level Output Disable Time	5		_	65	195	
$\overline{EO}_2$ , $\overline{EO}_4 \rightarrow On$ (L)	10	t <sub>PLZ</sub>	_	40	120	ns
	15			35	105	İ
High Level Output Enable Time	5			70	210	
$\overline{EO}_2$ , $\overline{EO}_4 \rightarrow On$ (H)	10	$t_{ ext{PZH}}$		35	105	ns
EO <sub>2</sub> , EO <sub>4</sub> →On (H)	15			30	90	
Low Level Output Enable Time	5			90	270	
$\overline{EO}_2$ , $\overline{EO}_4 \rightarrow On$ (L)	10	$t_{PZL}$		40	120	ns
EO <sub>2</sub> , EO <sub>4</sub> →On (L)	15			35	105	
Input Capacitance		Cı	_	_	7.5	pF

### • Switching Time Test Circuit and Waveforms

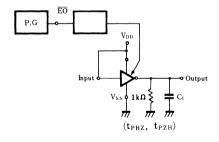
- [1]  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{THL}$ ,  $t_{TLH}$ 
  - 1. Test Circuit



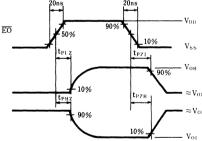
### 2. Waveforms

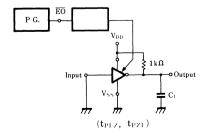


- [2]  $t_{PHZ},\ t_{PZH},\ t_{PLZ},\ t_{PZL}$ 
  - 1. Test Circuits



# 2. Waveforms





# $\blacksquare$ DC Characteristics $(V_{SS} \!=\! \! 0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=25℃		Ta=85℃		Unit
Itelli	(V)	bol		onations	min.	max.	min.	max.	min.	max.	Onn
Out and D	5					4	_	4	_	30	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		8		8	_	60	μA
	15					16		16	_	120	
	5		$V_I = V_{SS}$ or	37		0.05	_	0.05	-	0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	VDD	_	0.05	_	0.05	_	0.05	V
	15		$ 1_0  < 1\mu A$		_	0.05	_	0.05		0.05	
	5		V <sub>i</sub> =V <sub>SS</sub> or	17	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>		V DD	9.95	-	9.95		9.95		V
	15		$ I_0  < 1\mu A$		14.95		14.95		14.95	-	
	5			Vo=0.5V or 4.5V	_	1.5		1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3		3		3	V
	15		V <sub>0</sub> =1.5V or 13.5V		_	4	_	4	_	4	
	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	-	3.5	-	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1 \mu A$	Vo=1V or 9V	7		7		7	_	V
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11		11		
	4.75		$V_0 = 0.4V$	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I \!\!=\! 0 \text{ or } 10 \text{V}$	4.8		4		3.2	_	mA
Eow Bever	15		V <sub>0</sub> =1.5V,	$V_I = 0$ or $15V$	12		10		8	_	
	5		$V_0 = 4.6 V$	V <sub>I</sub> =0 or 5V	1		0.88		0.7		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5 V$	$V_I \!\!=\! 0 \text{ or } 10 \text{V}$	2.4		2.2		1.8	_	mA
	15		$V_0=13.5V, V_I=0 \text{ or } 15V$		6.6		6		4.8	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV		0.3		0.3	_	1	μA
3-State Leakage Current High Leve	15	Iozh	$V_0 = V_{DD}$		_	1.6		1.6	_	12	4
Output Pin Leakage Current Low Leve	15	-I <sub>ozL</sub>	$V_0 = V_{SS}$			1.6	_	1.6		12	μA

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0V,~C_L\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		_	35	105		
Output Rise Time	10	t <sub>TLH</sub>		20	60	ns	
	15			15	45		
	5		_	30	90		
Output Fall Time	10	t <sub>THL</sub>		15	45	ns	
	15			10	30		
Decreation Delay Time	5			80	240		
Propagation Delay Time In→On (H→L)	10	tPHL		35	105	ns	
In-On (H-L)	15			25	75		
Proposation Delay Time	5			65	195		
Propagation Delay Time In→On (L→H)	10	t <sub>PLH</sub>		30	90	ns	
In-On (L-H)	15		_	25	75		
High Level Output Disable Time $\overline{EO}_2$ , $\overline{EO}_4 \rightarrow On$ (H)	5		_	45	135		
	10	tPHZ		35	105	ns	
EU <sub>2</sub> , EU <sub>4</sub> →Un (H)	15	!		30	90		

# MN40098B/MN40098BS

### Hex Inverting 3-State Buffers

### Description

The MN40098B/S are hex inverting 3-state buffers which take large source and sink currents.

Two enable pins  $(\overline{EO}_2, \overline{EO}_4)$  are available which control 2 and 4 circuits independently.

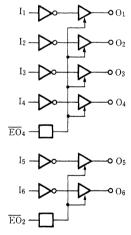
When  $\overline{EO_4}$  is "H", the output of buffers  $1 \sim 4$  becomes high impedance, adn when  $\overline{EO_2}$  becomes "H", the output of buffers  $5 \sim 6$  becomes high impedance.

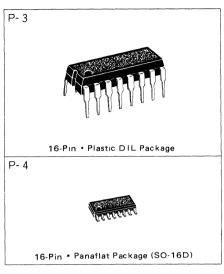
### Truth Table

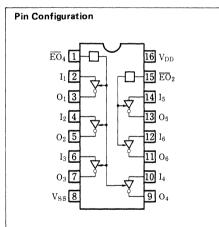
In	put	Output
I	EO	0
L	L	Н
Н	L	L
×	Н	high impedance

Note) X: don't care

### Logic Diagram







### ■ Maximum Ratings (Ta=25°C)

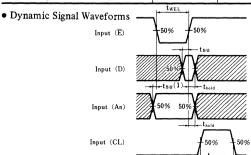
Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Input Current		$\pm\mathrm{I}_{\mathrm{I}}$	max. 10	mA	
Output Current		$\pm  I_{I}$	max. 25	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	***	
(per package) $T_a = +60 \sim +85^{\circ}$		$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (per output terminal)		$P_{D}$	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

<sup>\*</sup> VDD + 0.5V should be under 18V



### ■ Switching Characteristics $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$ (continued)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Propagation Delay Time	5		_	95	285	
•	10	t <sub>PLH</sub>	_	40	120	ns
$\overline{E} \rightarrow On (L \rightarrow H)$	15		_	30	90	
D D 1	5		_	95	285	
Propagation Delay Time	10	t <sub>PHL</sub>		35	105	ns
$D \rightarrow On (H \rightarrow L)$	15		_	25	75	
D. T.	5		_	85	255	
Propagation Delay Time	10	tplH	_	35	105	ns
$D \rightarrow On (L \rightarrow H)$	15		-	25	75	
December Delegation	5		-	110	330	
Propagation Delay Time	10	$t_{ ext{PHL}}$	_	45	135	ns
$An \rightarrow On (H \rightarrow L)$	15		-	35	105	
Propagation Delay Time	5		-	95	285	
	10	$t_{\rm PLH}$	_	40	120	ns
$An \rightarrow On (L \rightarrow H)$	15		_	30	90	
Propagation Delay Time CL→On (H→L)	5		_	85	255	
	10	$t_{ ext{PHL}}$	_	35	105	ns
	15		_	25	75	
Set-up Time	5		_	20	60	
D→E	10	tsu	_	5	20	ns
D→E	15		_	0	15	
Set-up Time	5		_	20	60	
-	10	tsu	_	10	25	ns
An→Ē	15		_	5	20	
II-14 Tim-	5		_	5	30	
Hold Time $D \rightarrow \overline{E}$	10	thold	_	5	20	ns
D→E	15		_	5	20	
Hold Time	5		_	25	75	
An→Ē	10	thold	_	10	30	ns
All→E	15		_	5	15	
	5		_	35	105	
Minimum $\overline{\overline{E}}$ Pulse Width	10	twel	_	15	45	ns
	15		_	10	30	
	5		_	35	105	
Minimum CL Pulse width	10	twclh	_	15	45	ns
	15		_	10	30	
Input Capacitance		Cı		_	7.5	pF



(1) The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

Waveforms showing minimum  $\overline{E}$  and CL pulse widths, set-up times, hold times, set-up and hold times are shown as positive values but may be specified as negative values.

### ■ Maximum Ratings (Ta=25°C)

### $*V_{DD} + 0.5V$ should be under 18V

Ite	m	Symbol	Ratings	Unit					
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V					
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V					
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V					
Peak Input · Output Current		$\pm I_{t}$	max. 10	mA					
Power Dissipation	Ta=-40~+60°C	D	max. 400	117					
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW					
Power Dissipation (1	per output terminal)	$P_{D}$	max. 100	mW					
Operating Ambient Temperature		Topr	-40~+85	°C					
Storage Temperature		Tstg	-65~+150	°C					

### $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

T4 a see	$V_{\mathrm{DD}}$	Sym-			Ta=-	- <b>40</b> ℃	Ta=	25℃	Ta=	<b>85</b> ℃	Limit
Item	(V)	bol	C	onditions	min.	max.	min.	max.	min.	max.	Unit
Onionant Barrer	5					20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	40	_	40	_	300	μA
- 11 /	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1 \mu A$	V <sub>DD</sub>	_	0.05		0.05	_	0.05	V
20 W 20 VOI	15		$ 1_0  < 1\mu A$		_	0.05		0.05		0.05	
	5		V — V	37	4.95		4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu \text{\AA}$	$V_{ m DD}$	9.95		9.95	_	9.95	_	V
	15		$ 10  < 1 \mu A$	:	14.95		14.95		14.95		
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5	-	1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$		3	_	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
Y 37-14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =1V or 9V	7	_	7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
	5		$V_0 = 0.4V$ ,	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5V$ ,	$V_l = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15V	3.6		3		2.4		
	5		$V_0 = 4.6V$ ,	$V_I = 0$ or $5V$	0.52		0.44	_	0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5V$ ,	$V_I$ =0 or 5V	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	V <sub>I</sub> =0 or 15	SV		0.3	_	0.3		1	μA

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\text{ , }V_{SS}\!=\!0\text{ V, }C_{L}\!=\!50pF)$

Item	$V_{\mathrm{DD}}\left( \mathrm{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	$\mathbf{t}_{\mathtt{THL}}$	_	30	90	ns
	15			20	60	
Propagation Delay Time	5		_	115	345	
Propagation Delay Time  E→On (H→L)	10	$t_{ ext{PHL}}$	_	50	150	ns
	15			35	105	



# MN4724B/MN4724BS

### 8-Bit Addressable Latches

### Description

The MN4724B/S are 8-bit addressable latches which have 1 common DATA input and 8 independent outputs. Each latch is controlled by 3-bit address input  $(A_0, A_1, A_2)$ .

When enable input  $(\overline{E})$  and clear input (CL) are "L", DATA is written in the bit selected by address input, and other bits maintain the previous mode.

When enable input  $(\overline{E})$  becomes "H", write-in to all bits is inhibited.

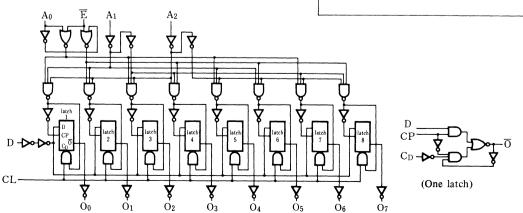
When enable input  $(\overline{E})$  and clear input (CL) are "H", all bits are reset to "L".

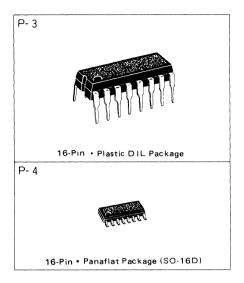
### Truth Table

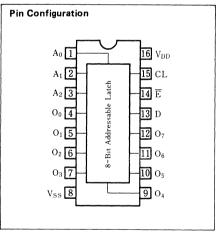
CL	Ē	D	A <sub>0</sub>	$A_1$	A <sub>2</sub>	O <sub>0</sub>	01	O <sub>2</sub>	O3	04	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	Mode
Н	Н	×	×	×	×	L	L	L	L	L	L	L	L	Clear
Н	L	D <sub>1</sub>	L	L	L	$D_1$	L	L	L	L	L	L	L	
Н	L	Dı	Н	L	L	L	$D_1$	L	L	L	L	L	L	
Н	L	Dı	L	Н	L	L	L	Dı	L	L	L	L	L	Non-
Н	L	D <sub>1</sub>	Н	Н	L	L	L	L	D <sub>1</sub>	L	L	L	L	specified
Н	L	Dı	L	L	Н	L	L	L	L	D <sub>1</sub>	L	L	L	latch is cleared.
Н	L	D <sub>1</sub>	Н	L	Н	L	L	L	L	L	$D_1$	L	L	Cicurou.
Н	L	D <sub>1</sub>	L	Н	Н	L	L	L	L	L	L	Dı	L	
Н	L	D <sub>1</sub>	Н	Н	Н	L	L	L	L	L	L	L	D <sub>1</sub>	
L	Н	×	×	×	×	On-1	Memory							
L	L	D <sub>1</sub>	L	L	L	D <sub>1</sub>	On-1	On-1	On-1	On-1	On-1	On-1	On-1	
L	L	Dı	Н	L	L	On-1	D <sub>1</sub>	On-1	On-1	On-1	On-1	On-1	On-1	Non-
L	L	D <sub>1</sub>	L	Н	L	On-1	On-1	D <sub>1</sub>	On-1	On-1	On-1	On-1	On-1	specified
L	L	D <sub>1</sub>	Н	Н	L	On-1	On-1	On-1	$D_1$	On-1	On-1	On-1	On-1	latch
L	L	D <sub>1</sub>	L	L	Н	On-1	On-1	On-1	On-1	D <sub>1</sub>	On-1	On-1	On-1	holds previous
L	L	D <sub>1</sub>	Н	L	Н	On-1	On-1	On-1	On-1	On-1	Dı	On-1	On-1	
L	L	D <sub>1</sub>	L	Н	Н	On-1	On-1	On-1	On-1	On-1	On-1	D <sub>1</sub>	On-1	
L	L	D <sub>1</sub>	Н	Н	Н	On-1	$D_1$							

Note) X: don't care;  $O_{n-1}:$  Mode before positive change of E  $D_{\iota}:$  H or L

### Truth Table



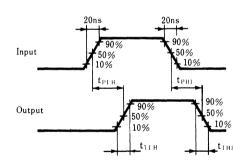




### 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	mın.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	$t_{TLH}$		30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
Propagation Delay Time	5			150	450	
An, Bn→On (L→H)	10	$t_{ ext{PLH}}$	_	60	180	ns
An, Bn→On (L→H)	15		_	45	135	
Propagation Delay Time	5			160	480	
An, Bn→On (H→L)	10	$t_{ ext{PHL}}$		65	195	ns
An, Dn→On (n→L)	15			45	135	
Propagation Delay Time	5			120	360	
In→On (L→H)	10	t <sub>PIH</sub>		50	150	ns
m→On (L→n)	15			35	105	
Propagation Delay Time	5			110	330	
	10	tPHI		45	135	ns
$In \rightarrow On (H \rightarrow L)$	15			30	90	
Input Capacitance		Cı		_	7.5	pF

### • Waveforms at Switching Time Test



### Condition Table (Example)

Condition 1a	ole (Exampl	.e)		
TEST	P.G.	Н	L	Output
An, Bn—On	D	$I_{A>B}$	Other	0
An, Dn—On	$\mathrm{B}_{\mathrm{0}}$	$I_{A=B}$	Input	O <sub>4&lt; B</sub>
T. O.	т		Other	0
In—On	$I_{A < B}$		Input	O <sub>A &lt; B</sub>

P.G.: Pulse Generator



### ■ Truth Table

			Input					Output	
	Comp	pare			Cascade			Output	
A <sub>3</sub> , B <sub>3</sub>	A2, B2	A <sub>1</sub> , B <sub>1</sub>	A <sub>0</sub> , B <sub>0</sub>	1a > b	1a < B	1 A = B	0a > b	0a < B	0a = B
$A_3>B_3$	×	×	×	Н	×	×	Н	L	L
$A_3 < B_3$	×	×	×	×	×	×	L	Н	L
$A_3 = B_3$	$A_2 > B_2$	×	×	Н	×	×	Н	L	L
$A_3 = B_3$	$A_2 < B_2$	×	×	×	×	×	L	Н	L
$A_3 = B_3$	$A_2 = B_2$	$A_1>B_1$	×	Н	×	×	Н	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	×	×	×	×	L	Н	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	Н	×	×	Н	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	×	×	×	L	Н	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	L	Н	L	L	Н
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	Н	L	L	Н	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	Н	L	L	Н	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	Н	Н	L	Н	Н
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	L	L	L

Note) X : don't care

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

	$V_{\mathrm{DD}}$	Sym-		_	Ta = -	-40℃	Ta=	25℃	Ta=	85℃	
Item	(V)	bol	(	Conditions	min.	max.	mın.	max,	min.	max.	Unit
	5					20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$		40		40		300	μA
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD		0.05		0.05		0.05	V
	15		$ 10  < 1\mu A$		_	0.05		0.05	_	0.05	
	5		$V_I = V_{SS}$ or	V	4.95		4.95		4.95		
Output Voltage High Level	10	$V_{OH}$		$\mathbf{v}_{\mathrm{DD}}$	9.95	-	9.95		9.95		V
	15		$ I_0  < 1\mu A$		14.95	_	14.95		14.95	_	
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$		1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1 \mu A$	Vo=1V or 9V	_	3		3		3	V
	15			Vo=1.5V or 13.5V		4	—	4		4	
T 37 1.	5			Vo=0.5V or 4.5V	3.5	-	3.5		3.5	-	
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4V$	$V_I = 0$ or $5V$	0.52		0.44	_	0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I = 0$ or $10V$	1.3	~	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15V	3.6		3	_	2.4		
	5		$V_0 = 4.6V$	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-J_{OH}$	$V_0 = 9.5 V$ ,	$V_l$ =0 or 10V	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	$V_{I}=0 \text{ or } 15V$	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7	_	1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_i = 0 \text{ or } 15$	SV -	_	0.3	_	0.3		1	μA

# MN4585B/MN4585BS

### 4-Bit Magnitude Comparators

### Description

The MN4585B/S are magnitude comparators which compare 4-bit input data  $A_0\sim A_4$  and  $B_0\sim B_3.$ 

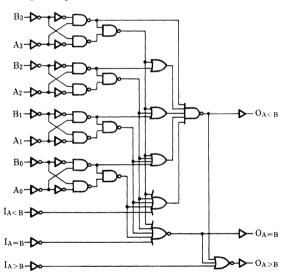
By using the MN4585B/S, large, small or equal signals can be obtained on the 3 output lines by the input (A < B, A = B, A > B). For the input more than 4-bit, a 4 X N bit comparator circuit can be composed by connecting a cascade input (A < B, A = B, A > B) of the MSB side and the output of LSB side.

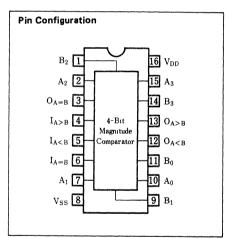
They are equivalent to MOTOROLA MC14585B.

# 16-Pin • Plastic DIL Package P- 4 16-Pin • Panaflat Package (SO-16D)

P- 3

### Logic Diagram





### Maximum Ratings (Ta=25℃)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	-0.5~+18	V
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_{i}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	357
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	೮
Storage Temperatur	е	Tstg	<b>−65~+150</b>	c

<sup>\*</sup> VDD + 0.5V should be under 18V

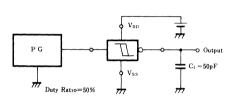


Switching Characteristics (Ta = 25%,  $V_{SS} = 0V$ ,  $C_L = 50pF$ ) (continued)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		1.5	2.2	_	
Threshold Voltage (Fig. 2)	10	VIL	3	4.5	_	V
	15		4	6.5		
	5		0.5	0.8	_	
Hysteresis Voltage (Fig. 2)	10	V <sub>H</sub>	0.7	1.3		V
	15		0.9	1.8	_	
Input Capacitance		CI	-	_	7.5	pF

Fig. 1 Switching Time Test Circuit and Waveforms

### 1. Test Circuit



### 2. Waveforms

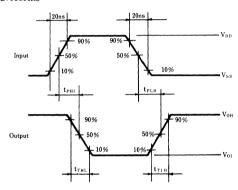
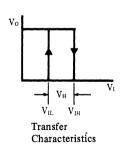
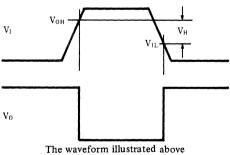


Fig. 2 Transfer Characteristics





The waveform illustrated above shows its definition rating 30%, to 70% limit.

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	
Item	(V)	bol	,	Conditions	min.	max.	min.	max.	min.	max.	Unit
<u> </u>	5				_	1		1		7.5	
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	2		2		15	μA
	15					4		4		30	
	5		$V_I = V_{SS}$ or	V	-	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_I - V_{SS} $ or $ I_O  < 1\mu A$	$v_{\mathrm{DD}}$	-	0.05		0.05	_	0.05	V
2011 20101	15		$ 1_0  < 1\mu A$			0.05		0.05		0.05	
	5		$V_I = V_{SSOT}$	V	4.95		4.95		4.95	~~~	
Output Voltage High Level	10	VoH	$ I_0  < 1\mu A$	V DD	9.95		9.95		9.95	_	V
	15		10  \ 1 \mu A		14.95	-	14.95		14.95		
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$		1.5		1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3		3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4		4	
T X7-1	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
0	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44	-	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5V$ ,	$V_I = 0$ or $10V$	1.3	_	1.1	-	0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6 V$ ,	$V_I$ =0 or 5 $V$	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4	_	
Output Current High Level	5	−I <sub>oн</sub>	$V_0 = 2.5 V$ ,	$V_I = 0 \text{ or } 5V$	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_I = 0$ or 15	SV .	_	0.3		0.3		1	μA

### 

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time (Fig. 1)	10	t <sub>TLH</sub>		30	90	ns
	15		_	20	60	
	5			60	180	
Output Fall Time (Fig. 1)	10	t <sub>THL</sub>		30	90	ns
	15			20	60	
	5			75	225	
Propagation Delay Time (Fig. 1)	10	$t_{\scriptscriptstyle \mathrm{PLH}}$		35	105	ns
	15			30	90	
	5		_	90	270	
Propagation Delay Time (Fig. 1)	10	$t_{ ext{PHL}}$		35	105	ns
	15			30	90	
	5		_	3.0	3.5	
Threshold Voltage (Fig. 2)	10	$V_{IH}$		5.8	7	v
	15			8.3	11	



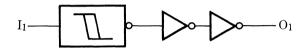
# MN4584B/MN4584BS

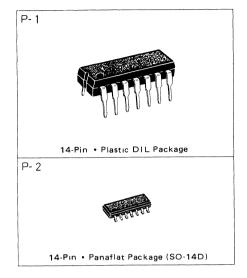
Hex Schmitt Triggers

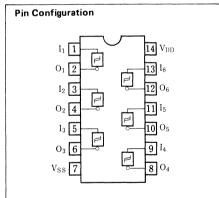
### Description

The MN4584B/S have hex waveform shaping circuits. They are used when high noise immunity is desired, and as waveform-shaping circuits to make late rise and fall time input. The MN4548B/S are equivalent to MOTOROLA MC14584B.

### ■ Logic Diagram (1/6)







### ■ Maximum Ratings (Ta=25°C)

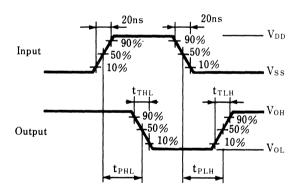
Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{ m DD}$	-0.5~+18	V
Input Voltage		$V_{I}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Outpu	t Current	± I1	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	W
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	ssipation (per output terminal) P <sub>D</sub>		max. 100	mW
Operating Ambient	Temperature	Topr	<b>−40~+85</b>	°C
Storage Temperatur	re	Tstg	$-65 \sim +150$	$^{\circ}$

<sup>\*</sup> VDD + 0.5V should be under 18V

### $\blacksquare$ Switching Characteristics $(Ta\!=\!25\%\,,~V_{SS}\!=\!0\,V,~C_{L}\!=\!50pF)$

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5		_	60	180		
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns	
	15		_	20	60		
Output Fall Time	5		-	60	180		
	10	t <sub>THL</sub>	_	30	90	ns	
	15		_	20	60		
Propagation Delay Time	5		_	130	390		
An→On (H→L)	10	$t_{ m PHL}$	_	50	150	ns	
An→On (H→L)	15		_	35	105		
Propagation Delay Time	5		_	105	315		
An→Ōn (L→H)	10	$t_{ ext{PLH}}$	_	40	120	ns	
An→On (L→H)	15		_	30	90		
Propagation Delay Time	5		_	120	360		
En→On (H→L)	10	t <sub>PHL</sub>	_	45	135	ns	
En-On (A-L)	15		_	30	90		
Propagation Delay Time	5			105	315		
En→On (L→H)	10	$t_{\rm PLH}$	_	40	120	ns	
Ell-Oll (L-II)	15		_	30	90		
Input Capacitance		Cı	_	_	7.5	pF	

### • Dynamic Signal Waveforms





### ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit		
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V		
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V.		
Output Voltage		$V_{O}$	$-0.5 \sim V_{DD} + 0.5^*$	V		
Peak Input · Output	Current	$\pm I_1$	max. 10	mA		
Power Dissipation	Ta=-40~+60℃	D	max. 400	117		
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW		
Power Dissipation (p	per output terminal)	$P_{D}$	max. 100	mW		
Operating Ambient	Temperature	Topr	-40~+85	°C		
Storage Temperatur	e	Tstg	Tstg −65~+150			

 $<sup>*</sup>V_{DD} + 0.5V$  should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS}=0V)$

Itam	$V_{\mathrm{DD}}$	Sym-		` d.k	Та=-	-40℃	Ta=25℃		Та=	85℃	Unit	
Item	(V)	bol	(	Conditions	mın	max.	min.	max.	mın.	max.	Unit	
Ouiescent Power	5			,	_	20	_	20		150		
Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$	_	40	-	40		300	μA	
	15					80		80	_	600		
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05		0.05	_	0.05		
Output Voltage Low Level	10	$V_{OL}$	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	_	0.05		0.05	_	0.05	V	
	15		$ 10  < 1 \mu A$			0.05	-	0.05	_	0.05		
Outroot Walt	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95		4.95		4.95	-		
Output Voltage High Level	10	Voh	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	9.95	_	9.95	and the same	9.95		V	
	15		10  < 1μA		14.95	_	14.95		14.95	_		
Y X7 1.	5		$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5		1.5		
Input Voltage Low Level	10	$V_{IL}$		Vo=1V or 9V	_	3	_	3		3	V	
	15			V <sub>0</sub> =1.5V or 13.5V	_	4		4	_	4		
Input Voltage	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5	_		
High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V	
	15			Vo=1.5V or 13.5V	11	_	11	_	11	_		
	5		$V_0 = 0.4V$ ,	$V_I = 0$ or $5V$	0.52		0.44	-	0.36			
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I$ =0 or 10V	1.3		1.1		0.9	_	mA	
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4	_		
0 0	5		$V_0 = 4.6V$ ,	$V_I = 0$ or $5V$	0.52		0.44	_	0.36	_		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I$ =0 or 10 $V$	1.3	_	1.1		0.9	_	mA	
	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6	_	3	_	2.4			
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1		mA	
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	5V		0.3		0.3	_	1	μA	

# MN4556B/MN4556BS

### Dual Binary to 1-of-4 Decoders

### Description

The MN4556B/S have dual decoder/demultiplexers. When enable input  $\overline{E} = L$ , one output of 4  $(\overline{O}_0, \overline{O}_1, \overline{O}_2 \text{ and } \overline{O}_3)$  is selected by two binary inputs  $(A_0 \text{ and } A_1)$ .

When enable input E = H, selection is inhibited and all outputs become "H".

Four-bit binary is decoded to hexadecimal by bit expanision, and also converted to many kind of codes.

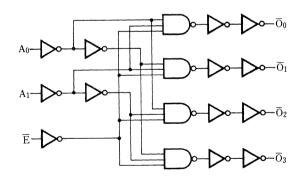
The MN4556B/S are equivalent to MOTOROLA MC14556B and RCA CD4556B.

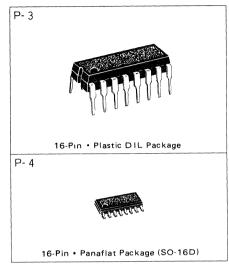
### Truth Table

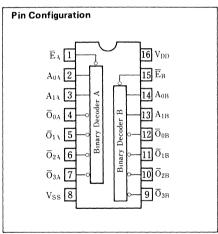
	Input		Output						
Ē	A <sub>0</sub>	$\mathbf{A}_1$	$\overline{O}_0$	$\overline{\overline{O}}_i$	$\overline{\overline{\mathrm{O}}}_{\mathtt{z}}$	$\overline{O}_3$			
L	L	L	L	Н	Н	Н			
L	Н	L	H	L	Н	Н			
L	L	Н	Н	Н	L	Н			
L	Н	Н	Н	Н	Н	L			
Н	×	×	Н	Н	Н	Н			

Note) X: don't care

### Logic Diagram (1/2)

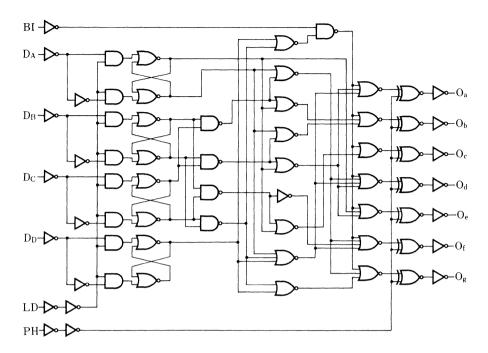








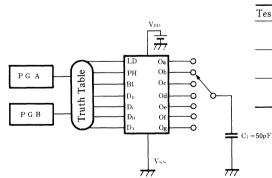
### Logic Diagram



### Switching Characteristics $(Ta = 25^{\circ}C, V_{SS} = 0V, C_{L} = 50pF)$

Item	$V_{\mathrm{DD}}\left(V\right)$	Şymbol	min.	typ.	max.	Unit	
	5			60	180		
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns	
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns	
	15			20	60		
Propagation Delay Time	5		_	180	540		
	10	t <sub>PHL</sub>		75	225	ns	
$Dn \rightarrow On (H \rightarrow L)$	15			55	165		
Propagation Delay Time	5			180	540		
	10	t <sub>PI H</sub>	_	75	225	ns	
$Dn \rightarrow On (L \rightarrow H)$	15			55	165		
Propagation Delay Time	5			145	435		
	10	$t_{ m PHL}$	_	65	195	ns	
$BI \rightarrow On (H \rightarrow L)$	15		_	45	135		
Dramantian Dalam Time	5		_	125	375		
Propagation Delay Time	10	t <sub>PLH</sub>	_	55	165	ns	
$BI \rightarrow On \ (L \rightarrow H)$	15		_	40	120		
Set-up Time	5			20	60		
	10	tsu	_	5	20	ns	
Dn→LD	15		_	0	15		
IX 11 m'	5			-15	0		
Hold Time Dn→LD	10	thold	_	0	15	ns	
บп→∟บ	15		_	5	20		
	5			30	90		
Minimum LD Pulse Width	10	twlDH	_	15	45	ns	
	15		_	10	30		
Input Capacitance		Cı		_	7.5	pF	

### • Switching Time Test Circuit



### Condition Table (Example)

Test No.	Item	P.G. A	P.G. B	"H"	"L"
1	D <sub>A-D</sub> —On	$D_{C}$		$D_4$ , $D_B$ , $LD$	D <sub>D</sub> , BI, PH
2	$t_{ m WLDH} \ t_{ m su}, \ t_{ m hold}$	Dc	LD	D <sub>4</sub> , D <sub>B</sub>	D <sub>D</sub> , BI, PH
3	BI—On	ВІ		D <sub>4</sub> , D <sub>B</sub> , LD	$D_C$ , $D_D$ , $PH$



### ■ Maximum Ratings (Ta=25°C)

Item		Symbol	Ratings	Unit		
Supply Voltage		$ m V_{DD}$	-0.5~+18	V		
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V		
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V		
Peak Input · Output C	Current	$\pm I_{I}$	max. 10	mA		
Power Dissipation	Γa=-40~+60°C	D	max. 400	mW		
(per package)	Γa=+60~+85°C	$P_{D}$	Decrease up to 200mW rating at 8mW/°C			
Power Dissipation (pe	r output terminal)	$P_{\mathrm{D}}$	max. 100	mW		
Operating Ambient T	emperature	Topr	-40~+85	°C		
Storage Temperature		Tstg	Tstg −65~+150			

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

### $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

E Do Grandeteristics (VSS VV)												
Item	$V_{ m DD}$	Sym-	(	Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit	
Trem	(V)	bol			min.	max.	min.	max.	min.	max.	Omt	
0	5					20	_	20	_	150		
Quiescent Power Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	_	40	_	40		300	μA		
Tarpy amount	15			_	80	_	80		600			
	5		17 — 17	17		0.05		0.05		0.05		
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	$V_{ m DD}$		0.05	_	0.05	_	0.05	V	
EOW ECVCI	15		$ I_0  < 1\mu A$			0.05		0.05		0.05		
	5		37 37		4.95	_	4.95	_	4.95			
Output Voltage High Level	10	V <sub>OH</sub>	$V_I = V_{SS}$ or $V_{DD}$		9.95		9.95		9.95		V	
mgn Bever	15		$ I_0  < 1\mu A$		14.95		14.95		14.95			
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5		
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	-	3	_	3	V	
Eow Ecrei	15			V <sub>0</sub> =1.5V or 13.5V		4	_	4	-	4		
	5			Vo=0.5V or 4.5V	3.5	_	3.5	_	3.5			
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7		V	
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11			
	5		$V_0 = 0.4 V$	V <sub>1</sub> =0 or 5V	0.52	_	0.44	_	0.36	-		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$ ,	$V_I$ =0 or 10 $V$	1.3	_	1.1	_	0.9		mA	
Dow Devel	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3	_	2.4			
	5		$V_0 = 4.6 V$ ,	V <sub>I</sub> =0 or 5V	0.52		0.44		0.36	_		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0$ or $10 \mathrm{V}$	1.3		1.1		0.9		mA	
	15		$V_0 = 13.5 V$	, $V_I = 0$ or 15V	3.6		3		2.4			
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4	_	1.1	_	mA	
Input Leakage Current	15	$\pm I_{I}$	V <sub>i</sub> =0 or 15	SV .		0.3	_	0.3		1	μA	

# MN4543B/MN4543BS

### BCD-to-Seven Segment Decoder/Drivers

### Description

The MN4543B/S are BCD-to-seven segment decoder/drivers for liquid crystal display with BLANKING input, PHASE input and LATCH DISABLE input.

The combination of output logic level can be reversed.

PH (input), BI (blanking input) and LD (latch disable input) are available in addition to the BCD input.

PH performs phase reverse of the truth value table.

BI performs blanking display.

LD performs BCD code storage.

In order to perform liquid crystal display (LCD), a common square-wave pulse is applied to the back plane of the display device and phase input of the MN4543B/S, and the output pins should be connected to the LCD segment.

The display diagram in this catalog should be referred to for in formation regarding connection to an LED, incandescent lamp, gas discharge tube, fluorescnet lamp, etc. (except the LCD).

The MN4543B/S are used for the display driver of counters, DVM computers and calculators, watches and timers.

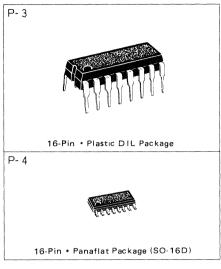
They are equivalent to MOTOROLA MC14543B.

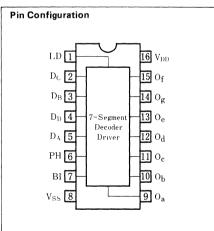
### Truth Table

		I	npu	l					0	utpu	t			Diamlari
LD	BI	РН	Dъ	Dc	Dв	DA	Oa	Ob	Ос	Od	Oe	Of	Og	Display
×	Н	L	×	×	×	×	L	L	L	L	L	L	L	blank
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	L	0
Н	L	L	L	L	L	Н	L	Н	Н	L	L	L	L	1
Н	L	L	L	L	Н	L	Н	Н	L	Н	Н	L	Н	2
Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
Н	L	L	L	Н	L	L	L	Н	Н	L	L	Н	Н	4
Н	L	L	L	Н	L	Н	Н	L	Н	Н	L	Н	Н	5
Н	L	L	L	Н	Н	L	Н	L	Н	Н	Н	Н	Н	6
Н	L	L	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
Н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
Н	L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	9
Н	L	L	Н	L	Н	L	L	L	L	L	L	L	L	blank
Н	L	L	Н	L	Н	Н	L	L	L	L	L	L	L	blank
Н	L	L	Н	Н	L	L	L	L	L	L	L	L	L	blank
Н	L	L	Н	Н	L	Н	L	L	L	L	L	L	L	blank
Н	L	L	Н	Н	Н	L	L	L	L	L	L	L	L	blank
Н	L	L	Н	Н	Н	Н	L	L	L	L	L	L	L	blank
L	L	L	×	×	×	×	**	**	**	**	**	**	**	**
dit	to	Н		dit	to		0	ppo	site	of a	bove	tab	le	ditto

Note) X: don't care

\*\* Previously added BCD defines at LD = H.





### ■ Segment Configuration



### Display

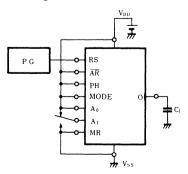




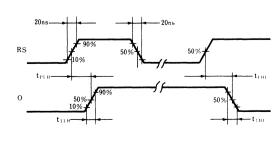
<sup>\*</sup> For LCD, square waveform is applied to PH. For a cathode common to LED, PH = L. PH = H at anode common LED.

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5			60	180		
Output Rise Time	10	t <sub>TLH</sub>		30	90	ns	
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns	
	15		_	20	60		
Propagation Delay Time	5		_	375	1125		
RS→O	10	t <sub>PHL</sub>		150	450	ns	
2 <sup>8</sup> selected	15	tPLH		110	330		
Propagation Delay Time	5			425	1275		
RS→O	10	t <sub>PHL</sub>		165	495	ns	
2 10 selected	15	t <sub>PLH</sub>		120	360		
Propagation Delay Time	5		_	510	1530		
RS→O	10	t <sub>PHL</sub>		190	570	ns	
2 13 selected	15	$t_{ m PLH}$		135	405		
Propagation Delay Time	5		_	575	1725		
RS→O	10	t <sub>PHL</sub>		210	630	ns	
2 16 selected	15	t <sub>PLH</sub>		150	450		
	5			30	90	ns	
Minimum Clock Pulse Width	10	twrst		15	45		
	15		_	12	36		
	5			30	90		
Minimum Reset Pulse Width	10	t <sub>wmrh</sub>		15	45	ns	
	15		_	12	36		
	5		8	16	_		
Maximum Clock Frequency	10	fmax	15	30	_	MHz	
	15		18	36			
$Rt = 5 k\Omega$	5	İ		90			
Oscillation Frequency Ct= 1 nF	10	$f_{osc}$	_	90		kHz	
$Rs = 10k\Omega$	15	""	_	90	_		
$Rt = 56k\Omega$	5		_	8	_		
Oscillation Ct 1 - F	10	fosc	_	8	_	kHz	
Frequency $Rs = 120k\Omega$	15			8			
Input Capacitance	<del>                                     </del>	Cı	_		7.5	pF	

### 1. Switching Time Test Circuit



### 2. Waveforms



# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage	Supply Voltage		-0.5~+18	V	
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		$V_0$	-0.5~V <sub>DD</sub> +0.5*	V	
eak Input · Output Current		± I1	max. 10	mA	
Power Dissipation	Ta=-40~+60°C	D	max. 400	117	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (per output terminal)		P <sub>D</sub>	max. 100	mW	
Operating Ambient Temperature		Topr	-40~+85	°C	
Storage Temperature		Tstg	-65~+150	°C	

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

•	$V_{\mathrm{DD}}$	Svm-		•••	Ta=-	-40℃	Ta=	25℃	Ta=	<b>85</b> ℃	Unit
Item	( <b>V</b> )	bol	C	onditions	min.	max.	min.	max.	min.	max.	Unit
_	5		D	_1.	_	20		20	_	150	
Quiescent Power Supply Current	10	$I_{\mathrm{DD}}$		Pın 5 = Hıgh Auto Reset Disabled		40	-	40		300	μA
Supply Current	15		Auto Kese	t Disabled	_	80		80		600	
Ouiescent Power	5		D: , 5 - D	ın 6 = Low	_	80		80	_	230	
Supply Current	10	$I_D$		Reset Enabled	_	750	_	600		700	μA
	15		rower On	Reset Enabled	-	1600		1300	_	1500	
Output Voltage	5		$V_1 = V_{SS}$ or	V		0.05		0.05		0.05	
Low Level	10	$V_{OL}$	$ I_0  < 1\mu A$	VDD	_	0.05	_	0.05	_	0.05	V
1			$ 10  < 1\mu A$		_	0.05		0.05		0.05	
Output Voltage	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95		4.95		4.95	_	
High Level	10	VoH	$ I_0  < 1\mu A$	v DD	9.95		9.95	•	9.95		V
	15		$ 10  < 1\mu A$		14.95		14.95		14.95		
Input Voltage	5			$V_0 = 0.5 V \text{ or } 4.5 V$	_	1.5		1.5		1.5	
Low Level	10	VIL	$ I_{\rm O} $ $<$ $1\mu{\rm A}$	$V_0=1V$ or $9V$	_	3		3		3	V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$		4		4		4	
Input Voltage	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	$V_0 = 1V$ or $9V$	7	_	7		7		V
	15			$V_0 = 1.5 V \text{ or } 13.5 V$	11		11		11		
Output Current	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.33		0.27	_	0.20	_	
$\begin{array}{c} \text{Low Level} \\ (C_{TC} = R_{TC} = Low) \end{array}$	10	$I_{OL}$	$V_0 = 0.5 V$ ,	$V_I {=} 0 \text{ or } 10 \mathrm{V}$	1.00	_	0.85		0.68		mA
	15		$V_0=1.5V$ ,	$V_I = 0$ or $15V$	3.20		2.70		2.30		
Output Current	5		$V_0=4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.5	_	0.4		0.3		
High Level $(C_{TG} = R_{TG} = H_1gh)$	10	-I <sub>OH</sub>	$V_0 = 9.5 V$ ,	$V_I {=} 0 \text{ or } 10 \text{V}$	1.4		1.2		0.95	_	mA
	15		$V_0 = 13.5 V_1$	, V <sub>1</sub> =0 or 15V	4.8		4,0		3.2	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>1</sub> =0 or 5V	1.4		1.2		0.95		mA
Input Leakage Current	15	$\pm I_1$	$V_{\rm I} = 0 \text{ or } 15$	V		0.3	_	0.3		1	μA



# MN4541B/MN4541BS

# Programmable Timers

#### Description

The MN4541B/S are programmable timers composed of a 16-stage binary counter, oscillator, automatic power-on reset circuit, output control and logic.

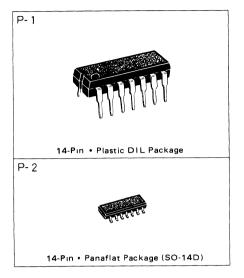
Timing starts at power ON. Counter starts its operation by the automatic reset when  $V_{\mbox{\scriptsize DD}}$  is in the specified range.

When the power is ON, external reset pulses can be applied. When the initial reset command is released, the oscillator operates by the frequency defined by the external RC network.

Each stage of the 16-stage counter divides the oscillator frequency into  $2^N$  squares.

The external master reset operates independently of automatic reset, and rise and fall of clock time is very late operation due to the built-in clock circuit.

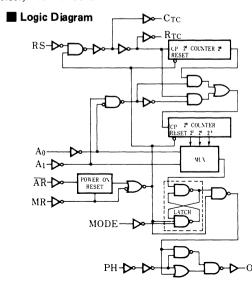
They are equivalent to MOTOROLA MC14541B.

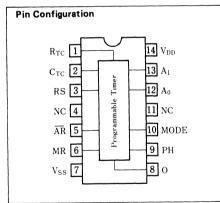


#### Truth Table

	Inp	out		Mode					
ĀR	MR	PH	MODE	Mode					
Н	L	×	×	auto reset impossible					
L	L	×	×	auto reset					
×	Н	×	×	reset					
×	L	×	Н	recycle mode					
×	L	×	L	single cycle mode					
×	L	L	×	first "L" output after reset					
×	L	Н	×	first "H" output after reset					

Note) X : don't care





#### Pin Explanation

 $A_0, A_1$ : Address input MODE: Mode select input

AR: Reset input MR: Reset input PH: Phase input

 $R_{\text{TC}}$ : External resistor  $(R_t)$  connection pin  $C_{\text{TC}}$ : External capacitance  $(C_t)$  connection pin RS: External resistor  $(R_S)$ , or external clock

input

Frequency Table

A <sub>0</sub>	$A_1$	Count Stage Number (n)	Count (2 <sup>n</sup> )			
L	L	13	8,192			
L	Н	10	1,024			
Н	L	8	256			
Н	Н	16	65,536			

# 

Item	$V_{\mathrm{DD}}\left( \mathbf{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>ri H</sub>	_	30	90	ns
	15			20	60	a E
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		-	120	360	
In→On (L→H)	10	t <sub>PI H</sub>	_	50	150	ns
In-On (L-H)	15		_	35	105	
Propagation Delay Time In→On (H→L)	5		-	120	360	
	10	t <sub>PHI</sub>	_	45	135	ns
	15			30	90	
Propagation Delay Time	5			155	465	
Sn→On (L→H)	10	t <sub>PIH</sub>		60	180	ns
Sil-Oii (L-H)	15		_	40	120	
Propagation Delay Time	5		_	165	495	
Sn→On (H→L)	10	t <sub>PHI</sub>		65	195	ns
Sn→On (n→L)	15			40	120	
Propagation Delay Time	5		_	100	300	
En→On (L→H)	10	$t_{\rm PLH}$	_	40	120	ns
Ell—On (L—n)	15			30	90	
Propagation Delay Time	5		_	100	300	
Ēn→On (H→L)	10	t <sub>PHI</sub>	_	40	120	ns
En→On (n→L)	15			30	90	
Input Capacitance		Cı	_	_	7.5	pF



# ■ Maximum Ratings (Ta=25°C)

Item	1	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	$-0.5 \sim +18$	V
Input Voltage		Vi	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		± I <sub>1</sub>	max. 10	mA
Power Dissipation	Ta=-40~+60°C	n	max. 400	117
(per package)	Ta=+60~+85°C	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (p	er output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	<b>−40~+85</b>	c
Storage Temperature		Tstg	$-65 \sim +150$	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

T	$V_{\mathrm{DD}}$	Sym-	,	Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	**
Item	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
Ouiescent Power	5				_	20	_	20	_	150	
Supply Current	10	$I_{DD}$	$V_l = V_{SS}$ or	$V_{DD}$		40	_	40		300	μA
	15				_	80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05	_	0.05	-	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1 \mu A$	VDD	-	0.05		0.05	_	0.05	V
	15		$ 10  < 1\mu A$			0.05		0.05		0.05	
0 + 47 +	5		V-V on	$V_1 = V_{SS}$ or $V_{DD}$			4.95		4.95		
Output Voltage High Level	10	V <sub>OH</sub>	$ I_0  < 1\mu A$	VDD	9.95		9.95		9.95		V
-	15		10  < 1μΛ		14.95		14.95	-	14.95		
	5			Vo=0.5V or 4.5V		1.5		1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_{O}  < 1\mu A$	Vo=1V or 9V	_	3	_	3		3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4	_	4	
Input Voltage	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	3.5	_	3.5		3.5		
High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7		7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11	_	11		11		
0 0	5		$V_0=0.4V$	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5 V$	$V_I {=} 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9		mA
	15		$V_0 = 1.5 V_1$	$V_I$ =0 or 15 $V$	3.6		3		2.4		
Outroot Co	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 13.5 V$	$=13.5V, V_I=0 \text{ or } 15V$		_	3		2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	$V_I = 0 \text{ or } 5V$	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	SV	_	0.3		0.3	_	1	μA

# MN4539B/MN4539BS

# Dual 4-Input Multiplexers

#### Description

The MN4539B/S are 4-channel data selectors which select data inputs by common select inputs  $(S_0, S_1)$ .

Each input of the two circuits appears at the outputs by the combination of select inputs during High enable input.

A Low at enable input forces outputs Low, independent of any other inputs. Applications are such areas as signal synthesizers and parallel-to-serial conversions.

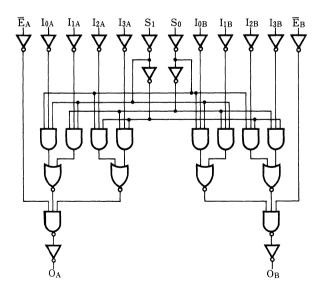
The MN4539B/S are equivalent to MOTOROLA MC14539B.

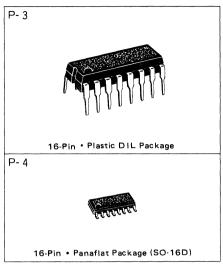
#### Truth Table

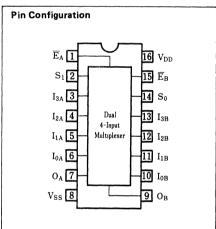
	Input						
So	Sı	Ē	0				
×	×	Н	L				
L	L	L	$I_{o}$				
Н	L	L	$I_1$				
L	Н	L	I <sub>2</sub>				
Н	Н	L	$I_3$				

Note) X: don't care

#### Logic Diagram







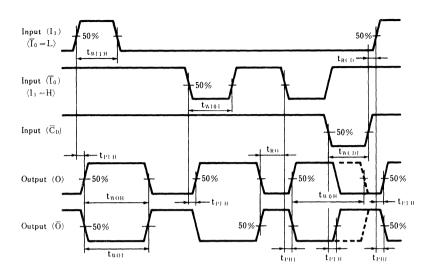
#### Pin Explanation

 $I_{0A}$ ,  $I_{1A}$ ,  $I_{2A}$ ,  $I_{3A}$ : Multiplexer input  $I_{0B}$ ,  $I_{1B}$ ,  $I_{2B}$ ,  $I_{3B}$ : Multiplexer input

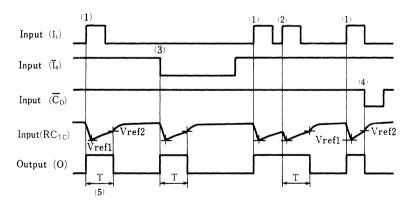
 $\begin{array}{ll} S_0,\ S_1\ :\ \mbox{Select input}\\ \overline{E}_A,\ \overline{E}_B\ :\ \mbox{Enable input}\\ O_A,\ O_B\ :\ \mbox{Multiplexer output} \end{array}$ 



#### • Dynamic Signal Waveforms



#### Timing Diagram



- (1) Positive edge truggering
- $(2)\ Positive\ edge\ re-triggering(pulse\ lengthening)$
- (3) Negative edge triggering
- (4) Reset (pulse shortening)
- (5)  $T=Rt\times Ct$

# $\blacksquare$ Switching Characteristics $\,(Ta\!=\!25\%\,,\ V_{SS}\!=\!0\,V,\ C_L\!=\!50pF)\,$

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	tTLH	_	30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
	5			150	450	
Propagation Delay Time	10	t <sub>PHL</sub>	_	70	210	ns
$\overline{I}_0$ , $I_1 \rightarrow O$	15			40	120	
D. T.	5		_	150	450	
Propagation Delay Time	10	t <sub>PLH</sub>	_	70	210	ns
$\overline{I}_0$ , $I_1 \rightarrow \overline{O}$	15	1 111		40	120	
	5			150	450	
Propagation Delay Time	10	t <sub>PHL</sub>		70	210	ns
$\overline{C}_{1} \rightarrow 0$	15	VIAL.	_	40	120	
	5			150	450	
Propagation Delay Time	10	t <sub>PLH</sub>	_	70	210	ns
$\overline{C}_0 \rightarrow \overline{O}$	15	LP1.H	_	40	120	5
	5	<del> </del>		0		
Recovery Time	10	tRCD	Montena	0	_	ns
$\overline{C}_0 \rightarrow \overline{I}_0$ , $I_1$	15	CRCD		0		115
	5	-		0		
Recovery Time	10			0		no
O, $\overline{O} \rightarrow \overline{I}_0$ , $I_1$	1	t <sub>RO</sub>		0		ns
	15			<del></del>		
Mınimum Pulse Width				60	180	
$\overline{\Gamma}_0$	10	t <sub>W101</sub>		30	90	ns
	15	ļ		20	60	
Minimum Pulse Width	5		_	60	180	
$I_1$	10	twill.		30	90	ns
	15	-		20	60	
Minimum Pulse Width	5		_	40	120	
$\overline{C}_{\mathrm{D}}$	10	twoDL		20	60	ns
	15			15	45	
Output Pulse Width	5			208	_	
$(Rt = 100k\Omega, Ct = 0.002\mu F)$	10	t <sub>wo</sub>	_	208		$\mu_{ extsf{S}}$
	15			208	<del></del>	
Output Pulse Width	5		_	10.4	_	
(Rt=100k $\Omega$ , Ct=0.1 $\mu$ F)	10	t <sub>WO</sub>		10.4	_	ns
, , , , , , , , , , , , , , , , , , , ,	15		*****	10.4	_	
Output Pulse Width	5		_	1.04	_	
$(Rt=100k\Omega, Ct=10\mu F)$	10	t <sub>WO</sub>	_	1.04		s
	15		_	1.04	_	
Input Capacitance		CI			7.5	pF
External Timing Resistance		Rt	5		1000	kΩ
External Timing Capacitance		Ct	2000	_	no limit	pF



# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage	Input Voltage		$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		±Ι <sub>Ι</sub>	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	$\mathbf{P}_{\mathrm{D}}$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)		Pp	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	<b>−65~+150</b>	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

## $\blacksquare$ DC Characteristics $(V_{SS}=0V)$

•	$V_{\mathrm{DD}}$	Svm-			Ta=-	-40℃	Ta=25℃		Ta=85℃		
Item	(V)	bol	C	Conditions	min.	max.	min.	max.	mın.	max.	Unit
Outescent Power	5				_	20		20	_	150	
Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
	15					80		80	_	600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	_	0.05	_	0.05		0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	VDD	_	0.05		0.05	_	0.05	V
	15		10  < 1 mA			0.05		0.05		0.05	
Outros Value	5		V-V an	$V_1 = V_{SS}$ or $V_{DD}$			4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{l} = V_{SS}$ or $V_{DD}$ $ I_{O}  < 1 \mu A$		9.95		9.95		9.95	_	V
	15		10  \ 1 \mu A		14.95		14.95		14.95		
¥ ¥7 f.	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_{O}  < 1\mu A$	Vo=1V or 9V		3		3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Innut Valtaga	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5	_	
Input Voltage High Level	10	V <sub>IH</sub>	$ I_{\rm O}  < 1\mu A$	$V_0 = 1V \text{ or } 9V$	7		7	_	7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11		11		
	5		$V_0 = 0.4V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I {=} 0 \text{ or } 10 \text{V}$	1.3		1.1	_	0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
0	5		$V_0 = 4.6 V$	$V_I = 0 \text{ or } 5V$	0.52	_	0.44	_	0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5 $V$	1.7		1.4		1.1	_	mA
Input Leakage Current	15	$\pm I_I$	$V_l = 0$ or 15	SV	_	0.3		0.3		1	μA

# MN4538B/MN4538BS

## Dual Precision Monostable Multivibrators

#### Description

The MN4538B/S are monostable multivibrators with the capability of reset and re-trigger.

Trigger can be performed from both the positive and negative going edge of the input pulse.

A wide range of precise output pulses can be obtained since the width and precision of the output pulse are defined by external  $C_{t}$  and  $R_{t}$ .

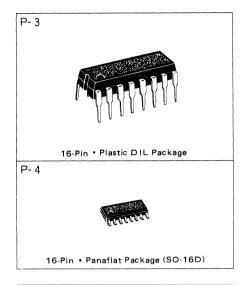
Output pulse width control is more precisely performed, due to linear CMOS technology.

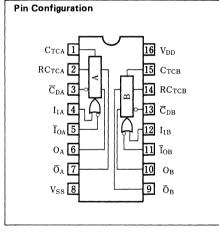
Total power supply voltage range is obtained as  $t_{WO}$  =  $R_r \cdot C_t$  and no other coefficient is included.

The MN4538B/S are equivalent to MOTOROLA MC14538B.

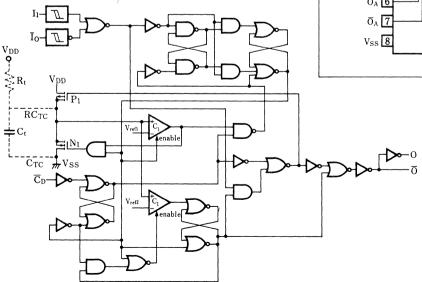
#### Truth Table

	Input	Output			
$\overline{\mathrm{I}}_{\mathrm{o}}$	$I_1$	$\overline{C}_{D}$	0	ō	
_	L	Н	Л	П	
Н		Н	Л	IJ	
×	×	L	L	Н	





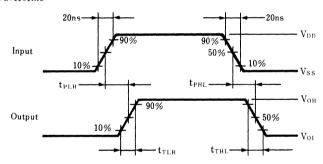
#### Logic Diagram (1/2)



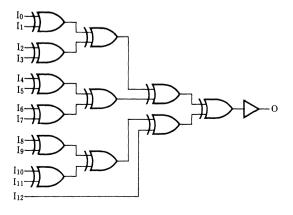


Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	tTHL	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	145	435	
$I_0 \sim I_{11} \rightarrow O  (H \rightarrow L)$	10	t <sub>PHL</sub>		60	180	ns
	15		_	45	135	
Propagation Delay Time	5		_	135	405	
$I_0 \sim I_{11} \rightarrow O  (L \rightarrow H)$	10	t <sub>PLH</sub>	_	55	165	ns
10 -111-0 (L-n)	15			45	135	
Propagation Delay Time	5			105	315	
I <sub>12</sub> →O (H→L)	10	t <sub>PHL</sub>	_	45	135	ns
112-0 (11-12)	15		_	35	105	
Propagation Delay Time	5		_	85	255	
I <sub>12</sub> →O (L→H)	10	tPLH	_	35	105	ns
	15		_	25	75	
Input Capacitance		Cı	_	_	7.5	pF

# • Dynamic Signal Waveforms



## Logic Diagram



# Maximum Ratings $(Ta=25^{\circ}C)$

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>1</sub>	-0.5~V <sub>DD</sub> +0.5*	V
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output	t Current	$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	317
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient	Temperature	re Topr -40~+85		°C
Storage Temperatur	re	Tstg	-65~+150	C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{DD}$	Sym-		Conditions	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	85℃	T.T
item	(V)	bol		Conditions		max.	min.	max.	min.	max.	Unit
Quiescent Power Supply Current	5 10	$I_{DD}$	$V_1 = V_{SS}$ or $V_{DD}$			20 40		20 40	_	150 300	μA
output	15					80		80		600	
Output Voltage	5 10	17	V <sub>I</sub> =V <sub>SS</sub> or	$V_{DD}$		0.05	_	0.05		0.05	v
Low Level	15	V <sub>OL</sub>	$ I_0  < 1\mu A$			0.05		0.05	_	0.05	V
Output Voltage High Level	5 10	Von	$V_I = V_{SS}$ or	$V_{DD}$	4.95 9.95		4.95 9.95	_	4.95 9.95	_	v
	15	1011	$ I_0  < 1\mu A$		14.95	-	14.95		14.95	_	·
	5			V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =1V or 9V		3	-	3	_	3	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
Input Voltage	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5	_	3.5	_	
High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	V <sub>0</sub> =1V or 9V	7		7	_	7	-	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
Output Current	5		,	$V_I = 0$ or $5V$	0.52		0.44		0.36	-	
Low Level	10	I <sub>OL</sub>	,	$V_I = 0$ or $10V$	1.3	_	1.1		0.9		mA
	15			V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current	5			$V_I = 0$ or $5V$	0.52		0.44	_	0.36		
High Level	10	−I <sub>OH</sub>	,	V <sub>I</sub> =0 or 10V	1.3	****	1.1		0.9		mA
	15		$V_0 = 13.5 V$	, V <sub>i</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0=2.5V$	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	5V		0.3		0.3	-	1	μA



# MN4531B/MN4531BS

12-Bit Parity Trees

#### Description

The MN4531B/S are 12-bit parity trees constructed with P and N channel enhancement modes.

The circle is composed of 12 data bit input  $(I_0 \sim I_{11})$  and an odd or even parity selection input  $(I_{12})$  and output (O).

This parity selection bit input is an added bit.

For words less than 12 bits, either even or odd parity output can be obtained depending on whether the other input is odd or even.

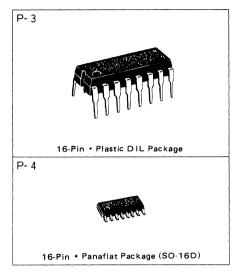
When the MN4531B/S are cascade-connected by using  $I_{12}$  input, more than 13-bit words can be processed.

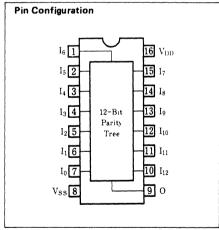
The MN4531B/S are widely used for error detection/correction systems of data, controllers for remote digital sensors, miuti arithmetic units without carry, etc.

#### Truth Table

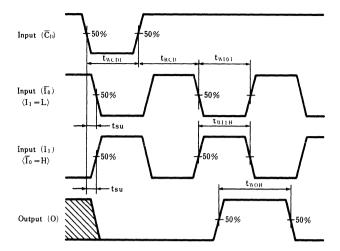
			1	nput					Output
I,2	I,,	I10		I,	I,	I,	Binary (Octod	ecimal)	0*
0	0	0		0	0	0	0	(0)	0
0	0	0		0	0	1	1	(1)	1
0	0	0		0	1	0	2	(2)	1
0	0	0		0	1	1	3	(3)	0
0	0	0		1	0	0	4	(4)	1
0	0	0		1	0	1	5	(5)	0
0	0	0		1	1	0	6	(6)	0
0	0	0		1	1	1	7	<b>(7</b> )	1
1	1	1		0	0	0	8184 (	17770)	0
1	1	1		0	0	1	8185 (	17771)	1
1	1	1		0	1	0	8186 (	17772)	1
1	1	1		0	1	1	8187 (	17773)	0
1	1	1		1	0	0	8188 (	17774)	1
1	1	1		1	0	1	8189 (	17775)	0
1	1	1		1	1	0	8190 (	17776)	0
1	1	1		1	1	1	8191 (	17777)	1

Note) \* 0 = Even Parity; 1 = Odd Parity





#### • Dynamic Signal Waveforms



Waveforms showing minimum  $\overline{\ I}_0$ ,  $I_1$  and O pulse widths, set-up and recovery times; set-up and recovery times are shown as positive values but may be specified as negative values.



■ Switching Characteristics  $(Ta = 25\%, V_{SS} = 0V, C_L = 50pF)$ 

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit	
	5	5,		60	180		
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns	
Output Rise Time	15	CTLH	_	20	60	5	
	5		<del> </del>	60	180	<del> </del>	
Output Fall Time	10		_	30	90	ns	
Output ran Time	15	t <sub>THL</sub>		20	60	115	
	5		<del></del>	155	465		
Propagation Delay Time	10			60	180		
$I_0$ , $I_1 \rightarrow O$		t <sub>PLH</sub>		1		ns	
	15	<u> </u>	<del></del>	40	120		
Propagation Delay Time	5		_	140	420		
$I_0, I_1 \rightarrow \overline{O}$	10	t <sub>PHL</sub>	_	50	150	ns	
	15	ļ		35	105		
Propagation Delay Time	5		_	105	315		
$C_{D} \rightarrow O$	10	t <sub>PHL</sub>	_	40	120	ns	
	15			30	90		
Propagation Delay Time $C_D \rightarrow \overline{O}$	5		_	120	360		
	10	t <sub>PLH</sub>	_	50	150	ns	
	15		_	35	105		
Minimum Pulse Width	5		_	25	75		
	10	twioL	_	15	45	ns	
$I_0$	15		_	10	30		
Minimum Pulse Width	5		_	25	75		
	10	twill	_	15	45	ns	
$I_1$	15		-	10	30		
	5		_	30	90		
Minimum Pulse Width	10	twcdL	_	15	45	ns	
$C_D$	15		_	10	30	{	
	5			235	_		
Output Pulse Width	10	twoH	_	155	_	ns	
$(Rt = 5 k\Omega, Ct = 15pF)$	15	1	_	140	_	1	
	5			5.45		<del> </del>	
Output Pulse Width	10	t <sub>woh</sub>	_	4.95	_	μs	
$(Rt=10k\Omega, Ct=1000pF)$	15	-won		4.85	_		
Input Capacitance		Cı			7.5	pF	
External Timing Resistance		Rt	5	_	1000	kΩ	
External Timing Capacitance (Note)		Ct			100	μF	
External runing Capacitance (NOte)	<u> </u>	_ Ci		L	10	$\mu_{\Gamma}$	

(Note) It is recommended to use the silicon diode (cathode toward  $V_{DD}$ ) in parallel with  $R_t$  when  $C_t$  is large capacity (ranging from  $0.1\mu F$  to  $10\mu F$ ).

# Truth Table

	Input		Out	put	Mode
I <sub>1</sub>	Īo	С́р	0	ō	Mode
	Н	Н	几		output pulse
	L	Н	L	Н	inhibit
Н	~	Н	L	Н	minor
L	_	Н	<u></u>		output pulse
×	×	L	L	Н	inhibit

Note) X : don't care

## ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit			
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V			
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	V			
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V			
Peak Input · Outpu	t Current	$\pm I_{I}$	max. 10	mA			
Power Dissipation	Ta=-40~+60°C	D	max. 400	11/			
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW			
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW			
Operating Ambient	ng Ambient Temperature		-40~+85	$^{\circ}$			
Storage Temperatur	re	Tstg	-65~+150	$^{\circ}$			

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{\rm SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	- <b>40</b> ℃	Та=	25℃	Ta=	85℃	Timia
Item	(V)	bol		onditions	min.	max.	min.	max.	min.	max.	Unit
0 :	5					20	_	20		150	
Quiescent Power Supply Current	10	$I_{DD}$	V <sub>I</sub> =V <sub>SS</sub> or V <sub>DD</sub>			40	_	40		300	μA
	15					80	_	80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	17	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol		V <sub>DD</sub>	_	0.05	-	0.05		0.05	v
	15		$ I_0  < 1\mu A$		_	0.05	_	0.05		0.05	
O	5		V-V	37	4.95		4.95		4.95		
Output Voltage High Level	10	Voh	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu A$	V <sub>DD</sub>	9.95		9.95		9.95		v
	15		10  < 1 µA		14.95	_	14.95	_	14.95		
	5			Vo=0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	_	3	_	3		3	v
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	_	4		4		4	
Toward N7 - 14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	VIH	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	_	7		V
	15			Vo=1.5V or 13.5V	11		11		11		
_	5		$V_0 = 0.4V$	$V_I$ =0 or 5V	0.52	_	0.44		0.36		
Output Current Low Level	10	$I_{OL}$	$V_0 = 0.5V$ ,	$V_I = 0 \text{ or } 10 \text{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6 V$	V <sub>i</sub> =0 or 5V	0.52		0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9	_ mA	mA
Ingli Dovel	15		$V_0 = 13.5 V$	, $V_I$ =0 or 15 $V$	3.6		3		2.4		
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7	_	1.4		1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_1 = 0 \text{ or } 15$	5V		0.3	_	0.3	_	1	μA



# MN4528B/MN4528BS

## Dual Monostable Multivibrators

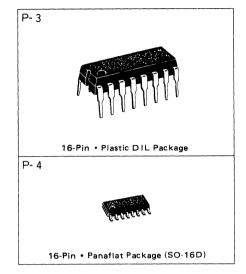
#### Description

The MN4528B/S are retriggerable, resettable monostable multivibrators and have 2 circuits in a package. The monostable pulse over a wide range of widths is determined by the external resistance and capacitance.

A negative going edge of the  $\overline{l_0}$  input when  $\overline{l_0}$  is Low or a positive going edge of the  $l_1$  input when  $\overline{l_0}$  is High produces a positive pulse at the O output and a negative pulse at the O output if the  $\overline{C_D}$  input is High.

A Low at the  $\overline{C_D}$  input forces the O output Low and the  $\overline{O}$  output High.

The MN4528B/S are equivalent to MOTOROLA MC14528B.



16 V<sub>DD</sub>

15 CextB

13 С<sub>рв</sub> 12 І<sub>ів</sub> 11 І<sub>ов</sub>

10 Ов 9 Ōв

 $C_{\text{ext}}/R_{\text{extB}}$ 

Pin Configuration

CextA

 $V_{SS}$  8

Cext/RextA 2

#### Pin Explanation

 $\bar{I}_{0A}$ ,  $\bar{I}_{0B}$ : Input (  $\searrow$  )  $I_{1A}$ ,  $I_{1B}$ : Input (  $\searrow$  )

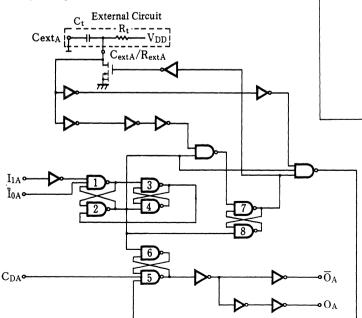
 $\overline{C}_{DA}$ ,  $\overline{C}_{DB}$ : Direct Clear Input

Cext<sub>A</sub>, Cext<sub>B</sub>: External capacitance connection

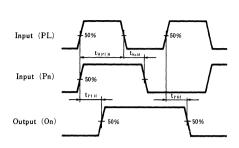
Cext/Rext<sub>A</sub>, Cext/Rext<sub>B</sub>: External capacitance, External resistance

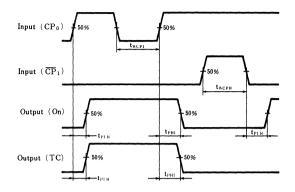
 $O_A$ ,  $O_B$ : Positive output  $\overline{O}_A$ ,  $\overline{O}_B$ : Negative output

## Logic Diagram (1/2)



#### • Dynamic Signal Waveforms

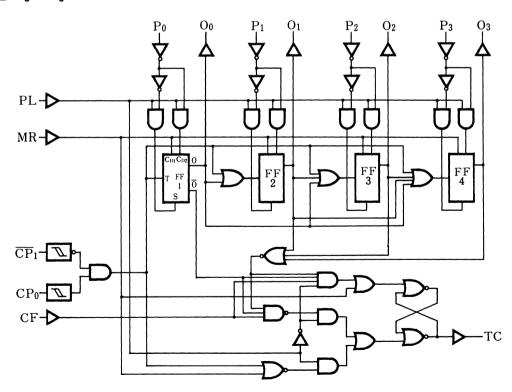




Waveforms showing minimum PL pulse width, propagation delays for PL,  $P_n$  to  $O_n$  and hold time for PL to  $P_n$ 

Waveforms showing minimum  $CP_0$  and  $\overline{CP}_1$  pulse widths, propagation delays for  $CP_0$  ,  $\overline{CP}_1$  to  $O_n$  and TC

#### ■ Logic Diagram





■ Switching Characteristics  $(Ta = 25^{\circ}C, V_{SS} = 0V, C_L = 50pF)$ 

Switching Characteristics	(1a-25C,	vss-uv, C	L=30pr)				
Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit	
	5			60	180		
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns	
	15		_	20	60		
	5		_	60	180		
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns	
	15	ļ		20	60		
Propagation Delay Time	5			150	450		
$CP_0$ , $\overline{CP}_1 \rightarrow On (H \rightarrow L)$	10	t <sub>PHL</sub>		65	195	ns	
	15	<u> </u>		50	150		
Propagation Delay Time	5			150	450		
$CP_0$ , $\overline{CP}_1 \rightarrow On (L \rightarrow H)$	10	t <sub>PLH</sub>		65	195	ns	
	15			50	150	-	
Propagation Delay Time	5			210	630		
$CP_0$ , $\overline{CP}_1 \rightarrow TC (H \rightarrow L)$	10	t <sub>PHL</sub>		90	270	ns	
	15	-	_	70 210	210 630	_	
Propagation Delay Time	10			90	270	ns	
$CP_0$ , $\overline{CP}_1 \rightarrow TC (L \rightarrow H)$	15	t <sub>PLH</sub>		70	210	115	
	5	-		200	600	<del> </del>	
Propagation Delay Time	10	t <sub>PHL</sub>		80	240	ns	
$PL \rightarrow On (H \rightarrow L)$	15	CPHL	_	60	180	5	
D 1 m'	5		_	180	540		
Propagation Delay Time	10	t <sub>PLH</sub>	_	70	210	ns	
$PL \rightarrow On (L \rightarrow H)$	15	1 211	_	50	150		
D D 1	5		_	140	420		
	10	t <sub>PHL</sub>	_	55	165	ns	
MR→On (H→L)	15		_	40	120		
	5		_	40	120		
ropagation Delay Time MR→On (H→L)  Iinimum CP <sub>0</sub> Pulse Width	10	twcpl	_	20	60	ns	
	15			15	45		
	5		_	40	120		
Minimum CP <sub>1</sub> Pulse Width	10	twcph		20	60	ns	
	15			15	45		
	5		_	50	150		
Minimum PL Pulse Width	10	twPLH	_	20	60	ns	
	15		_	16	48		
	5		_	65	195		
Minimum MR Pulse Width	10	twmrh	_	25	75	ns	
	15			20	60		
Hold Time	5		_	35	105		
Pn→ PL	10	thold	_	30	90	ns	
	15	-		25	75	<b></b>	
Maximum Clock Frequency	5		6	12	_		
(PL=L)	10	fmax	12	25	_	MHz	
	15		16	32			
Input Capacitance		Cı		_	7.5	pF	

# Maximum Ratings (Ta=25℃)

Ite	m	Symbol	Ratings	Unit	
Supply Voltage		$V_{DD}$	-0.5~+18	V	
Input Voltage		V <sub>I</sub>	$-0.5 \sim V_{DD} + 0.5^*$	V	
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V	
Peak Input · Output Current		± I <sub>1</sub>	max, 10	mA	
Power Dissipation	Ta=-40~+60℃	D	max. 400	117	
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW	
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW	
Operating Ambient	Temperature	Topr	-40~+85	°C	
Storage Temperatur	re	Tstg	-65~+150	°C	

<sup>\*</sup>V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	
nem	(V)	bol		Conditions	min.	max.	min.	max.	min.	max.	Unit
0	5					20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$	$V_{I} = V_{SS}$ or $V_{DD}$			40		40		300	μA
	15					80		80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	-	0.05	_	0.05	-	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	V DD		0.05		0.05		0.05	V
20.1.2.1.1	15		10  < 1 µA			0.05		0.05		0.05	
0	5		V <sub>I</sub> =V <sub>SS</sub> or	V	4.95		4.95	*****	4.95		
Output Voltage High Level	10	Voh	$ V_1 - V_{SS} $ or $ I_0  < 1 \mu A$	VDD	9.95	_	9.95		9.95	_	V
	15		1 <sub>0</sub>   < 1μΑ		14.95		14.95		14.95		
	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5	-	1.5	-	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_0  < 1\mu A$	V <sub>0</sub> =1V or 9V	_	3		3	_	3	v
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Input Voltage	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5		3.5		
High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7		7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		-
O	5		$V_0=0.4V$	$V_I$ =0 or 5V	0.52		0.44		0.36		
Output Current Low Level	10	I <sub>OL</sub>	$V_0 = 0.5 V$	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	V <sub>I</sub> =0 or 15V	3.6		3		2.4		
0	5		$V_0=4.6V$	$V_I$ =0 or 5V	0.52	_	0.44		0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5 V$	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
-	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	$V_I$ =0 or 5V	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_i = 0 \text{ or } 15$	iV .		0.3		0.3		1	μA



# MN4526B/MN4526BS

# Programmable 4-Bit Binary Counters

#### Description

The MN4526B/S are programmable 4-bit binary counters.

Cascade N dividing action can be performed by the cascade feedback input without an external gate.

They offer synchronization start of the N division cycle by a master reset function and disable of the pulse count function by the clock inhibit input.

The MN4526B/S are suitable for frequency division where low power dissipation and high noise immunity are desired, such as for frequency synthesizers and PLLs.

#### Count Mode

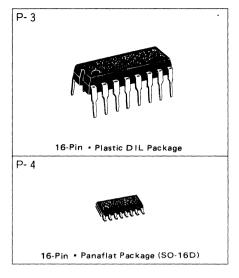
_		Out	put	
Count	О3	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>
15	Н	Н	Н	Н
14	Н	Н	Н	L
13	Н	Н	L	Н
12	Н	Н	L	L
11	Н	L	Н	Н
10	Н	L	Н	L
9	Н	L	L	Н
8	Н	L	L	L
7	L	Н	Н	Н
6	L	Н	Н	L
5	L	Н	L	Н
4	L	Н	L	L
3	L	L	Н	Н
2	L	L	Н	L
1	L	L	L	Н
0	L	L	L	L

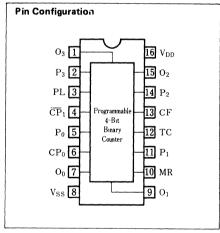
Note) CF = H; PL = L; MR = L

#### Truth Table

MR	PL	CP <sub>0</sub>	$\overline{\mathrm{CP}}_{\scriptscriptstyle 1}$	Mode
Н	×	×	×	reset (sync.)
L	Н	×	×	preset (sync.)
L	L		H	
L	L	L	~	no change
L	L	~	×	no change
L	L	×		
L	L		L	counter advance
L	L	Н		Counter advance

Note) X: don't care





#### Pin Explanation

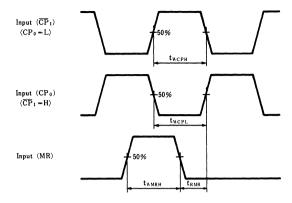
PL : Parallel load input  $P_0 \sim P_3$ : Parallel input

CF : Cascade feedback input  $CP_0$  : Clock input  $(L \rightarrow H)$   $\overline{CP}_1$  : Clock input  $(H \rightarrow L)$ 

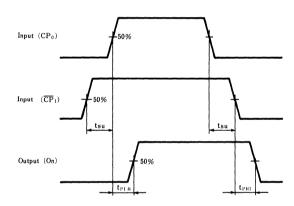
MR : Asynchronous master reset input

TC: Pin count output  $O_0 \sim O_3$ : Buffer parallel output

#### • Dynamic Signal Waveforms

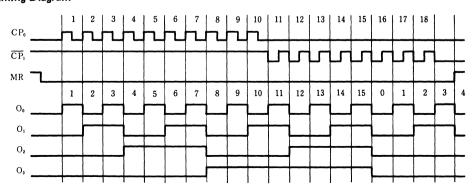


Waveforms showing recovery time for MR; minimum  $\text{CP}_0, \overline{\text{CP}}_1$  and MR pulse widths



Waveforms showing set-up times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to  $CP_0$  , and propagation delays

#### Timing Diagram





Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15		_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	145	435	
	10	t <sub>PLH</sub>		65	195	ns
$CP_0$ , $\overline{CP}_1 \rightarrow On (L \rightarrow H)$	15	}	_	50	150	
Propagation Delay Time	5		_	170	510	
	10	t <sub>PHL</sub>	_	75	225	ns
$CP_0$ , $\overline{CP}_1 \rightarrow On (H \rightarrow L)$	15		_	50	150	
Propagation Delay Time	5		_	145	435	
	10	$t_{ ext{PHL}}$	_	60	180	ns
$MR \rightarrow On (H \rightarrow L)$	15		_	45	135	
	5		_	85	255	
Low Level Minimum Clock CP <sub>0</sub> Pulse Width	10	twcpl	_	30	90	ns
	15		_	25	75	
	5		_	85	255	
High Level Minimum Clock CP <sub>1</sub> Pulse Width	10	twcph	_	30	90	ns
311 333	15		_	25	75	
	5		_	45	135	
High Level Minimum Reset Pulse Width	10	twmrh		20	60	ns
Table Water	15		_	15	45	
	5		_	25	75	
Reset Recovery Time	10	t <sub>RMR</sub>	_	15	45	ns
	15	1	_	10	30	
Set-up Time	5		_	90	270	
$CP_0 \rightarrow \overline{CP}_1$	10	tsu	_	35	105	ns
$CP_0 \rightarrow CP_1$	15			25	75	
Set-up Time	5		_	75	225	
Set-up Time $\overline{CP}_1 \rightarrow CP_0$	10	tsu	_	30	90	ns
Or 1→Or 0	15		_	20	60	
	5		3	6		
Maximum Clock Frequency	10	fmax	7	15		MHz
	15		10	21	_	
Input Capacitance		CI	_	_	7.5	pF

# **Maximum Ratings** (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		$V_{DD}$	-0.5~+18	v
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	v
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	v
Peak Input · Output Current		$\pm I_{I}$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	117
(per package)	Ta=+60~+85℃	$P_D$	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_D$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	ဗ
Storage Temperature		Tstg	<b>−65~+150</b>	r

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\begin{tabular}{ll} \blacksquare \begin{tabular}{ll} \textbf{DC Characteristics} & (V_{SS} = 0V) \\ \end{tabular}$

***	$V_{\mathrm{DD}}$	Sym-		4:4:	Ta=-	-40℃	Ta=	<b>25</b> ℃	Ta=	85℃	Unit
Item	(V)	bol	·	Conditions		max.	min.	max.	min.	max.	Unit
Quiescent Power	5				_	20	_	20		150	
Supply Current	10	$I_{DD}$	$V_I = V_{SS}$ or	$V_{DD}$		40		40		300	μA
	15					80	_	80		600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	V	NAME OF TAXABLE PARTY.	0.05	_	0.05	_	0.05	
Output Voltage Low Level	10	Vol	$ I_0  < 1\mu A$	<b>v</b> DD		0.05	_	0.05		0.05	V
	15		$ 1_0  < 1\mu A$			0.05		0.05		0.05	
0	5		V — V	37	4.95		4.95	_	4.95	-	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{\rm I} = V_{\rm SS}$ or $ I_{\rm O}  < 1 \mu { m A}$	$V_{\mathrm{DD}}$	9.95		9.95		9.95	-	V
	15		10  < 1μA		14.95		14.95		14.95	_	
	5			$V_0 = 0.5 V \text{ or } 4.5 V$		1.5	_	1.5		1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V		3	_	3	_	3	V
	15			V <sub>0</sub> =1.5V or 13.5V		4		4		4	
Y 4 37 - 14	5			$V_0 = 0.5 V \text{ or } 4.5 V$	3.5		3.5		3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	Vo=1V or 9V	7		7	-	7		V
	15			V <sub>0</sub> =1.5V or 13.5V	11		11	_	11		
	5		$V_0 = 0.4 V$	$V_I = 0$ or $5V$	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0 = 0.5 V$	$V_I$ =0 or 10V	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15V	3.6		3		2.4		
• • • •	5		$V_0 = 4.6V$ ,	$V_I = 0$ or $5\dot{V}$	0.52		0.44	_	0.36		
Output Current High Level	10	-I <sub>OH</sub>	$V_0 = 9.5V$ ,	$V_I$ =0 or 10V	1.3		1.1	_	0.9		mA
	15		$V_0 = 13.5V$	, V <sub>I</sub> =0 or 15V	3.6		3		2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4	_	1.1		mA
Input Leakage Current	15	$\pm I_{I}$	$V_i = 0 \text{ or } 15$	SV		0.3		0.3		1	μA



# MN4520B/MN4520BS

# Dual 4-Bit Binary Counters

#### Description

The MN4520B/S are dual 4-bit binary counters.

The counter advances on the positive going edge of the  $\overline{\text{CP}}_1$  when  $\overline{\text{CP}}_1$  is High or on the negative going edge of the  $\overline{\text{CP}}_1$  when the  $\text{CP}_0$  is Low.

A High on the reset input clears the counter (O  $_0\sim O_3$  = L). The MN4520B/S are equivalent to MOTOROLA MC14520B and RCA CD4520B.

#### Truth Table

Mode	MR	$\overline{\overline{\mathrm{CP_{\scriptscriptstyle 1}}}}$	CP <sub>0</sub>
counter advance	L	Н	
counter auvance	L	~	L
	L	×	
na shansa	L		×
no change	L	L	
	L	_	Н
$O_0 \sim O_3 = L$	Н	×	×

Note) X: don't care

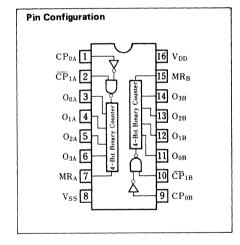
#### Pin Explanation

 $CP_{0A}$ ,  $CP_{0B}$ : Positive clock input (  $\checkmark$  )  $\overline{CP}_{1A}$ ,  $\overline{CP}_{1B}$ : Negative clock input (  $\searrow$  )

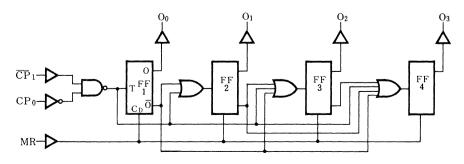
MRA, MRB: Reset input

 $O_{0A} \sim O_{3A}$  : BCD output (4 Bits)  $O_{0B} \sim O_{3B}$  : BCD output (4 Bits)

# P- 3 16-Pin • Plastic DIL Package P- 4 16-Pin • Panaflat Package (SO-16D)



#### Logic Diagram (1/2)



# 

Item	$V_{\mathrm{DD}}\left( \mathbf{V}\right)$	Symbol	min.	typ.	max.	Unit
	5		-	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5			60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15			20	60	
Propagation Delay Time An, Bn→On (H→L)	5		_	100	300	
	10	t <sub>PHL</sub>	_	45	135	ns
	15		_	35	105	
Propagation Delay Time	5			90	270	
An. Bn→On (L→H)	10	tplH	_	40	120	ns
An, Dn→On (L→n)	15		_	30	90	
Propagation Delay Time	5		_	95	285	
S <sub>A</sub> , S <sub>B</sub> →On (H→L)	10	t <sub>PHL</sub>		40	120	ns
$S_A$ , $S_B \rightarrow On (H \rightarrow L)$	15			30	90	
Proposition Dalay Time	5		_	85	255	
Propagation Delay Time	10	t <sub>PLH</sub>		40	120	ns
$S_A$ , $S_B \rightarrow On (L \rightarrow H)$	15		_	30	90	
Input Capacitance		Cı	-	_	7.5	pF



#### ■ Maximum Ratings (Ta=25°C)

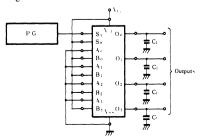
Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	$-0.5 \sim +18$	V
Input Voltage		$V_1$	$-0.5 \sim V_{DD} + 0.5^*$	I.
Output Voltage		$V_0$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60°C	D	max. 400	11.
(per package)	Ta=+60~+85℃	$P_{\rm D}$	Decrease up to 200mW rating at 8mW/°C	mW.
Power Dissipation (p	per output terminal)	P <sub>D</sub>	max. 100	mW.
Operating Ambient Temperature		Topr	-40~+85	°C
Storage Temperature		Tstg	$-65 \sim +150$	°C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

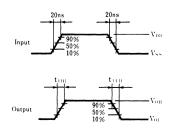
# $\blacksquare$ DC Characteristics $(V_{SS} = 0V)$

Item	$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40℃	Ta=	25℃	Ta=	85℃	Unit
	( V )	bol		Conditions	min.	max.	min.	max,	min.	max.	Omt
Quiescent Power	5				_	20	_	20	_	150	
Supply Current	10	$I_{DD}$	V <sub>i</sub> =V <sub>SS</sub> or	$V_{DD}$	_	40	-	40		300	μA
	15				_	80	_	80	_	600	
	5		V <sub>I</sub> =V <sub>SS</sub> or	7.	_	0.05		0.05		0.05	
Output Voltage Low Level	10	Vol	$ V_1 - V_{SS} $ or $ I_0  < 1\mu A$	VDD	_	0.05		0.05		0.05	V
	15		$ 10  < 1 \mu A$		_	0.05		0.05	_	0.05	
	5		X7 — X7	17	4.95		4.95		4.95	_	
Output Voltage High Level	10	Voh	$V_1 = V_{SS}$ or	V <sub>DD</sub>	9.95	-	9.95		9.95	_	V
	15		$ I_0  < 1\mu A$		14.95	_	14.95		14.95		
	5			$V_0 = 0.5 \text{V or } 4.5 \text{V}$		1.5		1.5	_	1.5	
Input Voltage Low Level	10	VIL	$ I_0  < 1\mu A$	Vo=1V or 9V	-	3		3	-	3	V
	15			V <sub>0</sub> =1.5V or 13.5V	_	4	-	4	_	4	
Immust Maltana	5			V <sub>0</sub> =0.5V or 4.5V	3.5	_	3.5	-	3.5	-	
Input Voltage High Level	10	$V_{IH}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	7	_	7		7		V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11	_	11		11		
	5		$V_0 = 0.4 V$ ,	$V_l = 0 \text{ or } 5V$	0.52	_	0.44		0.36	_	
Output Current Low Level	10	IoL	$V_0 = 0.5 V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3		1.1		0.9		mA
	15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3		2.4		
	5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5 $V$	0.52	_	0.44		0.36		
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5V$ ,	$V_I = 0 \text{ or } 10 \mathrm{V}$	1.3	_	1.1		0.9	-	mA
	15		$V_0 = 13.5 V_1$	, $V_I$ =0 or 15 $V$	3.6	_	3	_	2.4		
Output Current High Level	5	-I <sub>OH</sub>	$V_0 = 2.5 V$ ,	V <sub>I</sub> =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_i = 0 \text{ or } 15$	V .		0.3		0.3		1	μA

## 1. Switching Time Test Circuit



#### 2. Waveforms



# MN4519B/MN4519BS

# Quad 2-Input Multiplexers

#### Description

The MN4519B/S have following functions in one package.

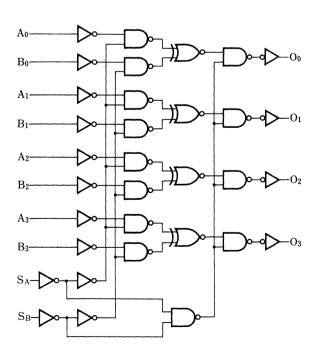
- \* 4-Bit AND/OR selector
- \* Quad 2-input data selector
- \* Quad Exclusive-NOR gate

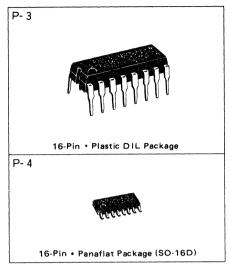
#### Truth Table

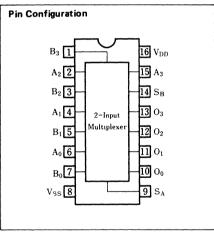
	Inp	out		Output
SA	Sв	An	B <sub>n</sub>	On
L	L	×	×	L
Н	L	An	×	An
L	Н	×	B <sub>n</sub>	$B_n$
Н	Н	L	L	H
Н	Н	Н	L	L
Н	Н	L	Н	L
Н	Н	Н	Н	Н

Note) X: don't care

#### Logic Diagram

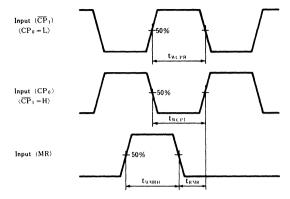




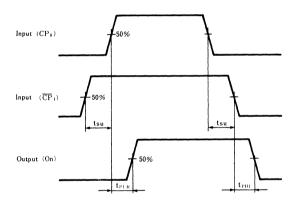




#### • Dynamic Signal Waveforms

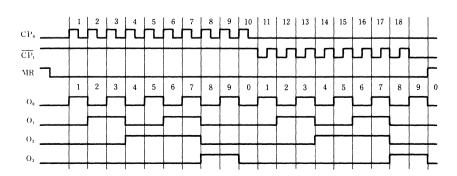


Waveforms showing recovery time for MR; minimum  $\text{CP}_0$  ,  $\overline{\text{CP}}_1$  and MR pulse widths



Waveforms showing set-up times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to  $CP_0$  , and propagation delays

#### Timing Diagram



# 

Item	$V_{\mathrm{DD}}\left(V\right)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15			20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	170	510	
$CP_0, \overline{CP}_1 \rightarrow On (H \rightarrow L)$	10	t <sub>PHI</sub>	_	75	225	ns
$CP_0, CP_1 \rightarrow On (H \rightarrow L)$	15		_	50	150	
Propagation Delay Time	5		_	145	335	
$CP_0, \overline{CP}_1 \rightarrow On (L \rightarrow H)$	10	t <sub>PLH</sub>	-	65	195	ns
	15		_	50	150	
Propagation Delay Time	5			145	335	
	10	t <sub>PHI</sub>		60	180	ns
MR→On (H→L)	15			45	135	
Minimum Clock CP <sub>0</sub> Pulse Width	5		_	85	255	
	10	twoPL	_	30	90	ns
	15		_	25	75	
	5		_	85	255	
Minimum Clock CP <sub>1</sub> Pulse Width	10	twcph		30	90	ns
77.10.01	15			25	75	
	5			45	135	
Minimum Reset Pulse Width	10	tww.	_	20	60	ns
	15		_	15	45	
	5		_	25	75	
Reset Recovery Time	10	$t_{RMR}$	_	15	45	ns
	15		_	10	30	
Set-up Time	5		_	90	270	
$CP_0 \rightarrow \overline{CP}_1$	10	tsu	_	35	105	ns
O1 0→OF 1	15			25	75	
Set-up Time	5		_	75	225	
$\overline{CP}_1 \rightarrow CP_0$	10	tsu	_	30	90	ns
011-010	15			20	60	
	5		3	6	_	
Maximum Clock Frequency	10	fmax	7	15	_	MHz
	15		10	21		
Input Capacitance		Cı	_	_	7.5	pF



# ■ Maximum Ratings (Ta=25°C)

Ite	m	Symbol	Ratings	Unit
Supply Voltage		$V_{\mathrm{DD}}$	-0.5~+18	V
Input Voltage		V <sub>I</sub>	-0.5~V <sub>DD</sub> +0.5*	V
Output Voltage		$V_{O}$	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_1$	max. 10	mA
Power Dissipation	Ta=-40~+60℃	D	max. 400	117
(per package)	Ta=+60~+85℃	P <sub>D</sub>	Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (	per output terminal)	$P_{D}$	max. 100	mW
Operating Ambient Temperature		Topr	-40~+85	C
Storage Temperature		Tstg	-65~+150	$^{\circ}$ C

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!\!0V)$

14	$V_{ m DD}$	Sym-			$T_a = -$	-40℃	Ta=25℃		Ta=85℃		Unit
Item	(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Cint
	5		$V_1 = V_{SS}$ or $V_{DD}$			20	_	20	_	150	
Quiescent Power Supply Current	10	$I_{DD}$				40	_	40	_	300	μA
outtry current	15					80	_	80		600	
	5		V – V	V		0.05		0.05	_	0.05	
Output Voltage Low Level	10	Vol	$V_I = V_{SS}$ or	V <sub>DD</sub>		0.05		0.05	_	0.05	V
Fow Fever	15		$ I_0  < 1\mu A$			0.05		0.05	_	0.05	
	5		V — V	17	4.95		4.95	_	4.95	_	
Output Voltage High Level	10	V <sub>OH</sub>	$V_{I} = V_{SS}$ or	$V_{\mathrm{DD}}$	9.95		9.95	_	9.95	_	V
21.6.1	15		$ I_0  < 1\mu A$		14.95		14.95		14.95		
	5			V <sub>0</sub> =0.5V or 4.5V		1.5		1.5	_	1.5	
Input Voltage Low Level	10	$V_{IL}$	$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V		3		3	_	3	v
20 2010.	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4	_	4	
7 . 77 1.	5			V <sub>0</sub> =0.5V or 4.5V	3.5		3.5	_	3.5		
Input Voltage High Level	10	$V_{IH}$	$ I_0  < 1\mu A$	$V_0 = 1V \text{ or } 9V$	7		7	_	7	_	V
	15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$	11		11		11		
	5		$V_0 = 0.4V$	$V_I = 0 \text{ or } 5V$	0.52		0.44		0.36		
Output Current Low Level	10	IoL	$V_0=0.5V$	$V_I = 0 \text{ or } 10 \text{V}$	1.3	_	1.1		0.9	_	mA
	15		$V_0 = 1.5 V$ ,	$V_I = 0 \text{ or } 15 \mathrm{V}$	3.6		3		2.4	_	
	5		$V_0 = 4.6V$ ,	$V_I = 0 \text{ or } 5V$	0.52		0.44	_	0.36	_	
Output Current High Level	10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I = 0$ or $10V$	1.3	_	1.1	_	0.9	_	mA
	15		$V_0 = 13.5 V$	, V <sub>I</sub> =0 or 15V	3.6		3	_	2.4	_	
Output Current High Level	5	$-I_{OH}$	$V_0 = 2.5 V$	$V_I$ =0 or 5V	1.7		1.4		1.1		mA
Input Leakage Current	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	V <sub>1</sub> =0 or 15V				0.3	_	1	μA

# MN4518B/MN4518BS

## Dual 4-Bit BCD Counters

#### Description

The MN4518B/S are dual BCD UP counters which enable count up to the second order of the BCD and division of the frequency.

All outputs  $(O_0 \sim O_3)$  become low during 1 High on the reset input, independent of the clock input. The counter advances on the positive going edge of the  $\overline{CP}_0$  when the  $\overline{CP}_1$  is High or on the negative going edge of the  $\overline{CP}_1$  when the  $CP_0$  is Low.

The MN4516B/S are equivalent to MOTOROLA MC14518B and RCA DE4518B.

#### Truth Table

$CP_{o}$	$\overline{\mathrm{CP}_{\scriptscriptstyle 1}}$	MR	Mode
	Н	L	counter advance
L	~	L	counter auvance
_	×	L	
×		L	
	L	L	no change
Н	_	L	
×	×	Н	$O_0 \sim O_3 = L$

Note) X: don't care

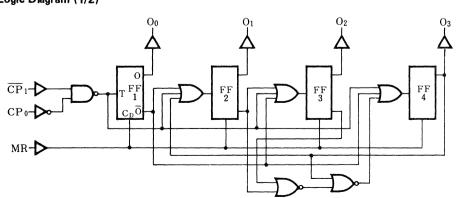
## Pin Explanation

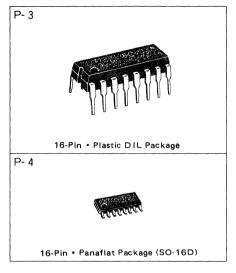
 $CP_{0A}$ ,  $CP_{0B}$ : Positive clock input (  $\bigcirc$  )  $\overline{CP}_{1A}$ ,  $\overline{CP}_{1B}$ : Negative clock input (  $\bigcirc$  )

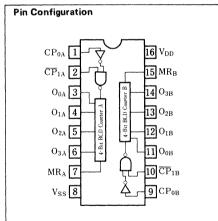
MRA, MRB: Reset input

 $O_{0A} \sim O_{3A}$  : BCD output (4 Bits)  $O_{0B} \sim O_{3B}$  : BCD output (4 Bits)

# Logic Diagram (1/2)



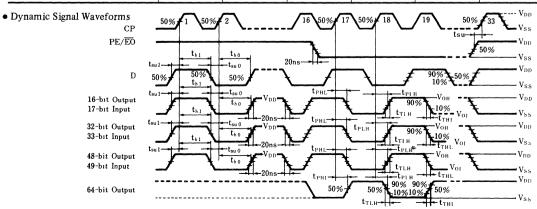






Switching Characteristics (Ta = 25%,  $V_{SS} = 0V$ ,  $C_L = 50pF$ )

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
	5		_	60	180	
Output Rise Time	10	t <sub>TLH</sub>	_	30	90	ns
	15	ļ	_	20	60	
	5		_	60	180	
Output Fall Time	10	t <sub>THL</sub>	_	30	90	ns
	15		_	20	60	
Propagation Delay Time	5		_	220	660	
<del>-</del> '	10	tPHL		85	255	ns
CP→On (H→L)	15		_	60	180	
D 1 T	5			190	570	
Propagation Delay Time CP→On (L→H)	10	t <sub>PLH</sub>	_	75	225	ns
	15		_	50	150	
	5			40	120	
High Level Output Disable Time $PE/\overline{EO} \rightarrow On  (H)$	10	t <sub>PHZ</sub>	_	30	90	ns
	15	1 112	_	25	75	
	5			50	150	
Low Level Output Disable Time	10	t <sub>PLZ</sub>		30	90	ns
$PE/\overline{EO} \rightarrow On (L)$	15	-1.22		25	75	
	5			45	135	
High Level Output Enable Time	10	t <sub>PZH</sub>	_	25	75	ns
PE/ <del>EO</del> →On (H)	15	1 211		20	60	
	5			60	180	
Low Level Output Enable Time	10	t <sub>PZL</sub>		30	90	ns
$PE/\overline{EO} \rightarrow On (L)$	15	J. Z.L		25	75	
	5	<b> </b>		10	30	
Set-up Time	10	tsu		5	25	ns
On, D→CP	15	-54	_	5	20	
	5			15	45	
Hold Time	10	thold	_	10	30	ns
On, D→CP	15	hold	_	10	25	115
	5		2	5		
Maximum Clock Frequency	10	fmax	6	12		MHz
manantani Clock i requestoy	15	Imax	8	16	_	WILLS
Input Capacitance	10	CI	- 0		7.5	pF



## Maximum Ratings (Ta=25℃)

Ite	m	Symbol	Ratings	Unit		
Supply Voltage		$V_{\mathrm{DD}}$	-0.5∼+18	V		
Input Voltage		Vi	$-0.5 \sim V_{DD} + 0.5^*$	V		
Output Voltage		Vo	$-0.5 \sim V_{DD} + 0.5^*$	V		
Peak Input · Output	Current	$\pm I_1$	max. 10	mA		
Power Dissipation Ta=-40~+6		D	max. 400	mW		
(per package)	Ta=+60~+85℃	$P_{D}$	Decrease up to 200mW rating at 8mW/°C	] mw		
Power Dissipation (p	er Dissipation (per output terminal) PD		max. 100	mW		
Operating Ambient	ent Temperature Topr		-40~+85	°C		
Storage Temperatur	e	Tstg	$-65 \sim +150$	°C		

<sup>\*</sup> V<sub>DD</sub> + 0.5V should be under 18V

# $\blacksquare$ DC Characteristics $(V_{SS}\!=\!0V)$

Item		$V_{\mathrm{DD}}$	Sym-		Conditions	Ta=-	-40°C	Ta=25℃		Ta=85℃		
		(V)	bol	Conditions		min.	max.	min.	max.	min.	max.	Unit
Quiescent Powe		5				_	50		50		375	
Supply Current	1	10	$I_{DD}$	$V_{\rm I} = V_{\rm SS} \text{ or}$	· V <sub>DD</sub>	_	100	_	100		700	μA
		15					200		200		1500	
Ontario V. Ir		5		V <sub>I</sub> =V <sub>SS</sub> or	. 17		0.05		0.05	_	0.05	
Output Voltage Low Level		10	Vol	$ I_0  < 1 \mu A$	VDD	_	0.05	_	0.05		0.05	v
		15		$ 10  < 1\mu A$			0.05	_	0.05	_	0.05	
0		5		V-V	17	4.95		4.95		4.95		
Output Voltage High Level		10	VoH	$egin{aligned} V_{ m I} = V_{ m SS} \  ext{or} \ V_{ m DD} \  I_{ m O}  < 1\mu ext{A} \end{aligned}$		9.95	_	9.95		9.95		v
		15				14.95		14.95		14.95	_	
* . ** *.		5	V <sub>IL</sub>   I		V <sub>0</sub> =0.5V or 4.5V	_	1.5	_	1.5		1.5	
Input Voltage Low Level		10		$ I_{\rm O}  < 1\mu A$	Vo=1V or 9V	_	3	_	3		3	v
		15			$V_0 = 1.5 \text{V or } 13.5 \text{V}$		4		4		4	
Immus Valsasa		5	V <sub>IH</sub>	$ I_0  < 1\mu A$	$V_0 = 0.5 V \text{ or } 4.5 V$	3.5	_	3.5		3.5		
Input Voltage High Level		10			Vo=1V or 9V	7		7		7		V
		15			Vo=1.5V or 13.5V	11		11		11		
0		5		$V_0 = 0.4V$ ,	$V_l = 0$ or $5V$	0.52	_	0.44	_	0.36	_	
Output Current Low Level		10	$I_{OL}$	$V_0=0.5V$ ,	$V_I = 0 \text{ or } 10V$	1.3		1.1		0.9	_	mA
		15		$V_0 = 1.5 V$ ,	$V_I$ =0 or 15 $V$	3.6		3	_	2.4		
0.4		5		$V_0 = 4.6V$ ,	$V_I$ =0 or 5 $V$	0.52	_	0.44		0.36	_	
Output Current High Level		10	$-I_{OH}$	$V_0 = 9.5 V$ ,	$V_I$ =0 or 10V	1.3	_	1.1	-	0.9		mA
		15		$V_0 = 13.5 V$	, $V_l$ =0 or 15 $V$	3.6	-	3		2.4		
Output Current High Level		5	$-I_{OH}$	$V_0 = 2.5 V$ ,	$V_I = 0 \text{ or } 5V$	1.7	_	1.4		1.1		mA
Input Leakage Curre	ent	15	$\pm I_I$	$V_1 = 0 \text{ or } 15$	iV .		0.3		0.3	_	1	μA
3-State Leakage Current	High Level	15	$I_{\rm OZH}$	$V_0 = V_{DD}$		_	1.6	_	1.6		12	^
Output Pin Leakage Current	Low Level	15	$-I_{\rm OZL}$	$V_o = V_{ss}$		_	1.6	_	1.6	-	12	μA

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# MN4517B/MN4517BS

# Dual 64-Bit Static Shift Registers

#### Description

The MN4517B/S are dual 64-bit static shift registers which have two independent 64-bit registers.

Each register can be used independently since they have their own clock input and write enable.

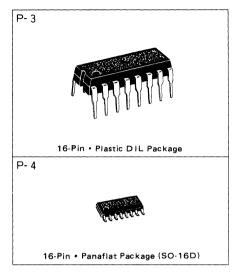
Outputs of 16, 32, 48 and 64 bits are available.

Data added in the data input is input to the register by clock regardless of the write enable input mode.

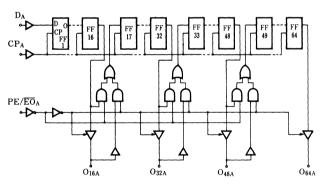
When wire enable input becomes "H" level, output becomes disable (high impedance mode), and when the clock pulse is applied, it is input to the input data 16, 32 and 48-bit tapes.

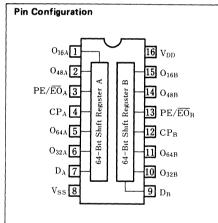
Accordingly, the contents of 64 bit is filled by 16 clock pulses. Tap output at every 16 bits can also be used for bus logic.

The MN4517B/S are used in time-delay circuits, tentative memory circuits, etc.



#### Logic Diagram



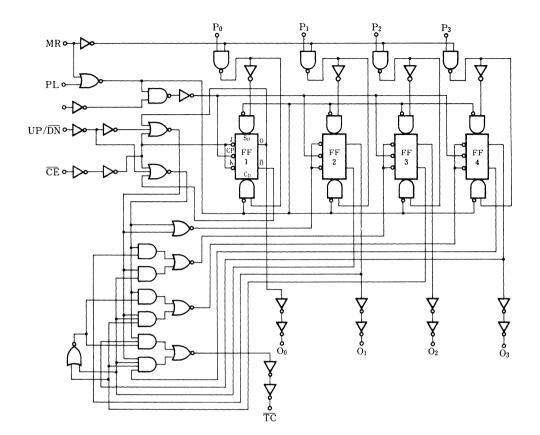


#### Truth Table

CP	PE/EO	D	O <sub>16</sub>	O <sub>32</sub>	O <sub>48</sub>	O <sub>64</sub>
0	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
0	1	×	High impedance	High impedance	High impedance	High impedance
1	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
1	1	×	High impedance	High impedance	High impedance	High impedance
	0	Enter into first bit	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit dispaly	Conternts of 64-bit display
	1	Enter into first bit	Data entering into 17th bit	Data entering into 33rd bit	Data entering into 49th bit	High impedance
_	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
	1	×	High impedance	High impedance	High impedance	High impedance

Note) X: don't care

# Logic Diagram





# CMOS Logic IC

# **MN4000B Series Data Book**

# MN4000B/MN4000BS Series

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